Panasonic

High Speed CMOS Logic MN74HC Series

Panasonic

Numerical and Functional Index

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Introduction to the CMOS Logic Family

The standard CMOS Logic Family has excellent characteristics such as low power dissipation, a wider range of operating power supply voltage, high noise margin, etc.; however, it has popularly been thought of as a medium speed element because the upper limit of the operating frequency is a few MHz at 5 V supply voltage compared to other standard logic families.

Matsushita Electronics Corporation has been conducting research and development of high-speed CMOS for application to high-speed electronic equipment as well, and has succeeded in the development of a new CMOS Logic family, the MN74HC Series, which has a pin configuration and operating speed in accordance with LS TTL.

Because of the standardized design of output drive characteristics, customers find system design easy by using the MN74HC Series, and the series will be expanded for applications to all electronic equipments for consumer and industry use.

For further applications of small and thin equipments, we have succeeded in supplying the Pana-flat package as the MN74HC00S Series. We are continually developing and introducing new products of high quality, high performance and high reliability, and we sincerely hope you will find this catalog for design engineers useful.

October, 1986

International Marketing Division Semiconductor Group Matsushiata Electronics Corporation

The circuit examples in this manual have been used to describe the characteristics and properties of these products. The contents of the manual are complete as far as necessary to assure accuracy and reliability, and Panasonic assumes no responsibility with respect to problems resulting from the use of the circuits described herein or patents by third persons. Specifications may also be changed without notice in order to make improvements.

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	NOR	MN74HC02,	MN74HC27,	MN74HC4002,	MN74HC4078	
	AND	MN74HC08,	MN74HC11,	MN74HC21		
	OR	MN74HC32,	MN74HC4075			
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Gates Buffers	Buffer	MN74HC367,	MN74HC540,	MN74HC541,	MN74HC4050,	MN74HC4306
Dullers		MN74HC04,	MN74HCU04,	MN74HCT04,	MN74HC240,	MN74HC366,
	Inverter	MN74HC368,	MN74HC4049,	MN74HC4305		
	Exclusive-OR	MN74HC86,	MN74HC386			
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Transceivers	 	MN74HC242,	MN47HC243,	MN74HC245,	MN74HC640,	MN74HC643
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DI: DI		MN74HC112,	MN74HC173,	MN74HC174,	MN74HC175,	MN74HC273,
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			MN74HC4303,	MN74HC4304		
		MN74HC75,	MN74HC77,	MN74HC373,	MN74HC375,	MN74HC533,
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	D.	MN74HC161,	MN74HC163,	MN74HC393,	MN74HC4020,	MN74HC4024,
Counters	Binary	MN74HC4040,	MN74HC4060,	MN74HCT4060,	MN74HC4520	
Decade		MN74HC160,	MN74HC162,	MN74HC390		
	Analog	MN74HC4051,	MN74HC4052,	MN74HC4053,	MN74HC4066	· · · · · · · · · · · · · · · · · · ·
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	Digital	MN74HC253,	MN74HC257,	MN74HC258,	MN74HC352,	MN74HC353
Encoders	4	MN74HC147,	MN74HC148			
Multivibrator		MN74HC221				
Comparator	· · · · · · · · · · · · · · · · · · ·	MN74HC688				·····
Others		MN74HC183,	MN74HC280,	MN74HCT280		



Descriptions

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Descriptions

1. Outline of MN74HC Series

where low-power dissipation, a wider range of supply voltage and high noise margins are required, featuring basic logical functions and complete compatibility with LS TTL in pin configuration and operating speed. Easy system design is possible because of the standardized design of output drive characteristics. The MN74HC Series consists of the MN74HCOO Series standard DIL package, and the MN74HCOOS Series, which has enabled smaller and thinner electronic equipment by adopting a small Pana-flat package.

The MN74HC Series is designed to be used in systems

* Features of the MN74HC Series

High-speed operation (V_{CC} 5V)
 Typical gate propagation delay times:
 t_{nd1} = 6 ns typ. (C_L = 15 pF)

$$t_{pd2}$$
 = 8 ns typ. (C_L = 50 pF)
Typical flip-flop operating frequency:
 f_{max} = 60MHz typ. (C_L = 50 pF)

- (2) Wider range of operating power supply voltage = 1.46 V
- ~ 6 V
 (3) Low power dissipation:

1.0 mW/Gate ($V_{CC}=5 \text{ V}, f_1=1 \text{MHz}, C_1=15 \text{ pF}$)

- (4) Wider operating temperature range: $-40 \sim +85^{\circ}$ C
- (5) High noise margin
- (6) Direct drive of LS TTL 10-input
- (7) Same function and same pin configuration as LS TTL 54/74 Series. Some have the same function and pin configuration as the CMOS 4000 Series.
- (8) Built-in static electricity protection circuitry

2. Comparison with Other Logic Families

Comparison between MN74HCOO (Quad 2-Input NAND Gates) and other logic families with same functions.

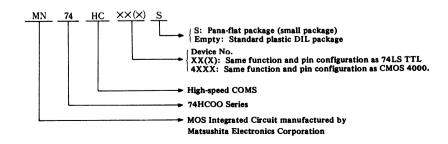
Parameter	H CMOS	LS TTL	TTL	B-Type CMOS	Remarks
Power Supply Voltage	1.4~6V	5±5%V	5±5%V	3∼15V	
Power Dissipation (typ.)	1mW/Gate	2mW/Gate	10mW/Gate	1mW/Gate	$V_{CC}=5V$, $C_L=15p$ $f_i=1 MHz$
Quiescent Power (max.)	100µ W/Gate	22mW/Gate	110mW/Gate	40µW/Gate	$V_{CC}=5V$, $V_{I}=GND$
Propagation Delay Time (typ.)	6ns	10ns	10ns	50~100ns	$V_{CC}=5V$, $C_L=15pI$
Output Current (I _{OL}) (min.)	2.5mA	8mA	16mA	0.36mA	V _{CC} =5V
Noise Margin	1 V	0.4V	0.4V	1 V	V _{CC} =5V
Operating Temperature	-40~+85℃	0~+70℃	0~+70℃	-40~+85℃	

Table 1 2-Input NAND Gate Comparison Chart

3. Ordering and Numbering System

The following indications information is needed for orders.

(Type Number)



4. Basic Circuitry and Construction of MN74HC MOS

The basic explanation gives, as an example, the inverter of the MN74HC Series.

As shown in Figure 1, the 74HC MOS inverter consists of a p-channel enhancement type MS transistor (P_1) and an n-channel enhancement type MOS transistor (N_1) . Input is made by commonly connecting each gate, and output is made by commonly connecting each drain.

 $V_{\rm CC}$ (+), is the source of the p-channel MOS transistor, and GND(-) is the source of the n-channel MOS transistor. In this figure, the voltage ($V_{\rm O}$) of the output (O) is considered when the voltage ($V_{\rm I}$) of input (I) changes from $V_{\rm CC}$ to GND

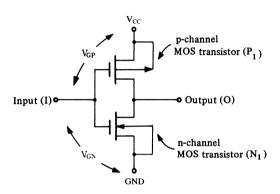


Fig. 1 74HC MOS Inverter

4.1 When input (1) is GND level

 V_{GP} (voltage between gate and source) of P_1 is $-(V_{CC}-GND)$, and P_1 switches ON because negative deep bias is applied to the gate. V_{GN} (voltage between gate and source) of N_1 is O, and N_1 becomes OFF. Output (O) becomes partial pressured level by the resistor ratio P_1 and N_1 but output voltage (V_O) becomes approximately V_{CC} because ON and OFF resistance become, respectively, tens of ohms and several hundreds of M ohms. In this instance, no current flows from V_{CC} to GND

4.2 When the input (1) is an intermediate level between V_{CC} and GND

 P_1 and N_1 become ON and output (O) becomes intermediate level partially pressured by P_1 ON and N_1 ON resistors. In this instance, output voltage $(V_{\rm O})$ becomes approximately $V_{\rm CC}$ and GND when the input voltage (V_1) is near the level of GND and $V_{\rm CC},$ respectively.

Current flows from V_{CC} to GND.

4.3 When the input (1) is V_{CC} level

When V_{GP} of P_1 and V_{GP} of N_1 are zero and $(V_{CC}-GND)$, P_1 and N_1 become OFF and ON, respectively. Accordingly, the operation becomes completely the reverse of the order in 4.1, the voltage (V_O) of output (O) becomes approximately GND level, and no current flows from V_{CC} to GND. The quadrature axis shows an input voltage and the axis of ordinates shows an output voltage in Fig. 2. The dotted line of the axis of ordinates shows current flowing from V_{CC} to GND; current flows (I_{CC}) only when the inverter changes.

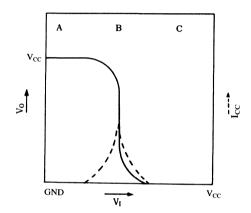


Fig. 2 74HC MOS Inverter Input/output Voltage Characteristics

A sectional view of the 74HC MOS inverter is shown in Fig. 3. There should be perfect separation between the p-channel and n-channel MOS transistors in order for the 74HC MOS inverter to be used on the signal silicon substrate; for this purpose, a pn conjunction is used.

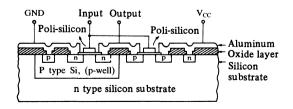
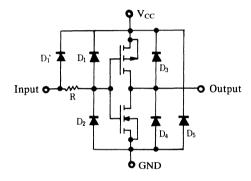


Fig. 3 Sectional view of the 74HC MOS inverter

In this figure, the p-channel MOS transistor is grown on the n type silicon substrate and the n-channel MOS transistor is grown on the p-well in the substrate. When power is switched on, the substrate and p-well become in a condition of reverse bias of $(V_{\rm CC}-{\rm GND})$, because the n-type substrate and p-well are connected to $V_{\rm CC}$ and GND respectively. Therefore, the p- and n-channel transistors can operate independently of each other. A parastic diode is inserted into the 74HC MOS circuit, as shown in Fig. 4, and, when the rating at each terminal is exceeded, excessive forward current may flow to these diodes, and the IC may be damaged. For this reason, absolute maximum ratings must be maintained.



R: Input protection diode

n.

 $D_{1'}$: Input protection diode

 D_2 :

D₃: p-channel transistor

Parasitic diode by drain growth

D₄: n-channel transistor

Parasitic diode by drain growth

D₅: Parasitic diode by p-well growth

Fig. 4. 74HC MOS inverter equivalent circuit considering parasitic element

As shown in Fig. 4, input protection diodes such as D_1 , D_1 , and D_2 are used for the protection of the CMOS input gate from static electricity. These diodes are used in all products of the MN74HCOO Series (although only D_2 is used in the MN74HC4049/S and MN74HC4050/S).

5. Handling of the MOS Device

Circuits for protection against static electricity are used in all MEC MOS ICs; however, the IC will be damaged by accidental excessively high voltage.

Accordingly, the following cautions should be followed in order to handle the device safely.

(1) During use

Be sure to ground the person (by a resistor of $1M\Omega$) handling the ICs and also any charged materials on the work discharged.

(2) For storage and transport

It is necessary to use an MEC – specified container and/or conductive material. These containers are used to either short or insulate ICs.

(3) Test and Handling

When testing and moving an IC from one carrier to another, be sure to handle it on a conductive board (metal table, etc.) Also be sure to ground the person to the conduction table (by a metal chain or lead wire). Testing and handling equipment should also be grounded to the metal table. A signal should not be input when the devices is in the OFF mode.

(4) Securing

It is necessary to secure the MOS IC after all parts have been secured, and it is best to ground the IC, the metal portion of the printed-circuit board, the jigs, tools and workers in order to prevent a failure in the process line.

If the printed-circuit board can't be grounded, the worker should first touch the printed-circuit board before he touches the MOS IC to the printed-circuit board.

(5) Soldering

The soldering iron, even a low-voltage one, and the soldering bath should also be grounded.

(6) Static electricity

Workers should wear clothes which do not attract static elecricity (avoid using work clothing made of nylon or other synthetic fibers). Care should be taken even after the MOS IC is secured to the printed-circuit board. Conductive clips or tape should be connected to the terminals of the circuit board in order to protect from static electricity through the board, because the board is only an extension of the lead wire of the device secured to the board until the assembled board is installed in the system and the appropriate voltage is applied.

6. Symbols and Terms

Current

+ is current flowing into an element and - is current flowing out from the element.

Symbol	Term	Description
II	Input current	Sink current at the specified input voltage and V _{CC}
Іон	Output HIGH current	Sink driving current at the specified output HIGH voltage and V_{CC}
I _{OL}	Output LOW current	Sink driving current at specified output LOW voltage and $V_{\rm CC}$
I _{CC}	Quiescent power supply current	Sink current into the V_{CC} terminal at the specified input voltage V_{CC}
I _{OZ}	Output OFF current	Current which flows into or out from an off-state tri-state output when the output is connected to V_{CC} or GND
I _{IL}	Input LOW current	Current which flows into an element at the specified input LOW voltage and V_{CC}
I _{IH}	Input HIGH current	Current which flows into an element at the specified input HIGH voltage and V_{CC}
I _{CCL}	Quiescent LOW power supply current	Current which flows into the $V_{\rm CC}$ terminal at the specified input LOW voltage and $V_{\rm CC}$ against all inputs
I _{CCH}	Quiescent HIGH power supply current	Current which flows into the V_{CC} terminal at the specified input HIGH voltage and V_{CC} against all terminals

Voltage

GND is the lowest voltage which is applied to an element; all voltages are relative in value to GND.

Symbol	Term	Description	
V _{cc}	Power supply voltage	Highest positive (+) voltage	
GND	Power supply voltage	Highest negative (-) voltage of a single power supply; reference voltage level to others; GND	
V _{EE}	Power supply voltage	One of the negative power supply voltages and highest negative power supply voltage which is a reference voltage to others	
V _{IH}	Input HIGH voltage	Input voltage range showing logical HIGH of the system	
V _{IL}	Input LOW voltage	Input voltage range showing logical LOW of the system	
V _{OH}	Output HIGH voltage	Voltage range of the output terminal at the specified output load and power supply voltage	
V _{OL}	Output LOW voltage	Voltage range of the output terminal at the specified output load and power supply voltage	

Analog symbol

Symbol	Term	Description
R _{ON}	ON resistance	Effective ON resistance of analog-transmission gate at the specified input voltage, output load and $V_{\rm CC}$
ΔR _{ON}	Δ ON resistance	Difference of effective ON resistance between the two transmission gates of the analog-switch at the specified input voltage, output load and $V_{\rm CC}$

Common Specifications



Common Specifications

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Common Specifications

High-speed CMOS logic IC MN74HCOO Series operates in the range of $V_{\rm CC}$ = + 1.4 \sim 6.0 V (GND=0V), and each specification is guaranteed at $V_{\rm CC}$ =2.0V, 4.5V and 6.0V.

The high-speed CMOS logic IC operates in the wider range; therefore, it is not so critical relative to power supply regulation as the conventional logic IC (TTL, LS TTL).

It operates at $V_{\rm CC}$ = +1.4 V (min.) if the noise margin and interfacing problem with other equipment are not considered.

In addition, it operates at $V_{\rm CC}$ = +6.0 V (max.) if power dissipation and interface are not considered. Unused terminals should be connected to $V_{\rm CC}$, GND or other input terminals. Countermeasures against static electricity are taken for the input/output terminals of the high-speed CMOS logic IC; however, we recommend careful handling even so.

Individual specifications are described in the individual data sheets; common specifications are summarized as follows.

1. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

	Paramet	er	Symbol	Rating	Unit	
Supply voltag	e		V _{cc}	-0.5~+7.0	V	
Input/output	voltage		V _I , V _O	-0.5~V _{CC} +0.5	V	
Input protect	ion diode current		I _{IK}	±20	mA	
Output parasi	tic diode current		I _{OK}	±20	mA	
Output curre	nt		Io	±25 (STD), ±35 (Bus driver)	mA	
Supply curren	nt		I _{CC} , I _{GND}	±50 (STD), ±70 (Bus driver)	mA	
Storage temp	erature range		Tstg	-65~+150	°C	
	MN74HCXX	Ta=-40~+60°C	D	400	mW	
Power	WIN /4HCAX	Ta=+60~+85°C	P _D	Decrease to 200mW at the rate of 8mW/°C		
dissipation	MN74HCXXS	Ta=-40~+60°C	ъ	275	mW	
		Ta=+60~+85°C	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	11144	

■ Operating Conditions

Parameter	Sumb al		Rating				
Farameter	Symbol	HC	HCU	НСТ	Unit		
Operating supply voltage	V _{cc}	1.4~6.0	1.4~6.0	4.5~5.5	V		
Input/output voltage	V _I , V _O	0~V _{cc}	0~V _{cc}	0~V _{cc}	v		
Operating temperature range	Ta	-40~+85	-40~+85	-40~+85	°C		
Input rise and fall time	t _r , t _f	(V _{CC}) 2.0V 0~1000 4.5V 0~500 6.0V 0~400	(V _{CC}) 2.0V 0~1000 4.5V 0~500 6.0V 0~400	0~500	ns		



2. Main Characteristic Figures

Necessary main characteristics are shown by the example of MN74HCOO (Quad 2-Input NAND Gates)

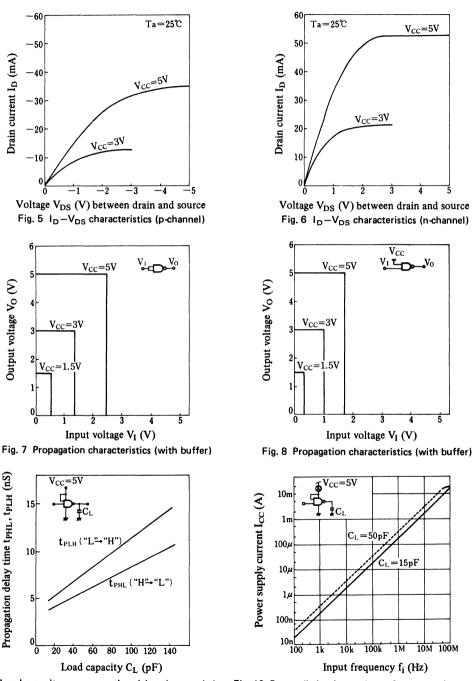


Fig. 9 Load capacity vs. propagation delay characteristics Fig. 10 Power dissipation vs. input frequency characteristics

3. DC characteristics (GND=0V)

Table 3 Characteristics

							haracte	ristics	T					
			Sym-	V_{CC}		Test Co					mperatu	· · · · · · · · · · · · · · · · · · ·		
Paramete	er		bol	(V)	Vı		Io		ļ	$Ta = 25^{\circ}$	<u>c</u>	Ta=-40)~+85°C	Unit
		Type			.,	STD	BUS	Unit	min.	typ.	max.	min.	max.	
				2.0					1.5			1.5		V
		HC		4.5					3.15			3.15		V
Input HIGH vol	tage		V _{IH}	6.0					4.2			4.2		V
		нст		4.5					2.0			2.0		v
				5.5					2.0			2.0		
				2.0							0.3		0.3	V
		HC		4.5							0.9		0.9	V
Input LOW volt	age		VIL	6.0							1.2		1.2	V
				4.5 [≀]			1				0.8		0.8	v
				5.5							0.0		0.0	
				2.0	1	-20.0	-20.0	μA	1.9	2.0		1.9		V
				4.5	V _{IH}	-20.0	-20.0	μA	4.4	4.5		4.4		V
		HC Voi		6.0	or	-20.0	-20.0	μA	5.9	6.0		5.9		V
Output HIGH v	oltage		Voh	4.5	VIL	-4.0	-6.0	mA	3.86			3.76		V
				6.0		-5.2	-7.8	mA	5.36			5.26		V
		HCT		4.5	V _{IH} or	-20.0	-20.0	μA	4.4	4.5		4.4		V
		1101		4.5	VIL	-4.0	-6.0	mA	3.86			3.76		V
				2.0		20.0	20.0	μA		0.0	0.1		0.1	V
				4.5	Vін	20.0	20.0	μΑ		0.0	0.1		0.1	V
		HC		6.0	or	20.0	20.0	μΑ		0.0	0.1		0.1	V
Output LOW vo	oltage		Vol	4.5	Vil	4.0	6.0	mA			0.32		0.37	V
				6.0		5.2	7.8	mA			0.32		0.37	V
		нст		4.5	V _{IH}	20.0	20.0	μA		0.0	0.1		0.1	V
		IIC I		4.5	or V _{IL}	4.0	6.0	mA			0.32		0.37	V
Input current		HC	II	6.0	V	V _{CC} or	CND				±0.1		±1.0	μΑ
input current		нст	11	5.5							±0.1		±1.0	μA
Analog switch		HC	Is	6.0	V_{I} =	V _{IH} or	V_{iL}				±0.1		±1.0	μA
OFF current		НСТ	15	5.5	V _S	$=V_{CC}$ o	r GND				±0.1		±1.0	μA
3-state output		HC	Ioz	6.0	V_{I} =	V _{IH} or	VIL				±0.5		±5.0	μA
Off state curren	nt	НСТ	1oz	5.5	$V_0 =$	V _{CC} or	GND				±0.5		±5.0	μA
	SSI	нс		6.0							2.0		20.0	μΑ
	~~.	НСТ		5.5	V ₁ = '	V _{CC} or	GND				2.0		20.0	μA
Quiescent		HC		6.0	1	• ((01	OND				4.0		40.0	μA
supply current	FF	НСТ	I_{CC}	5.5	$I_0 =$	$I_0 = 0$					4.0		40.0	μA
f		HC		6.0							8.0		80.0	μA
	MSI	нст	,	5.5						İ	8.0		80.0	μA
	1101		0.0	L					L	U. V	L			

4. AC Characteristics

Table 4 AC Switching · Parameter

Symbol	Description	Symbol	Description
fi	Input frequency	tw	Pulse width
fo	Output frequency	thold	Hold time
f max.	Maximum clock frequency	tsu	Set-up time
tr, tf	Clock input rise & fall time	tPHZ	3-state output disable time H→Z
tplH	Propagation time (propagation delay time) L→H	tPLZ	3-state output disable time L→Z
t _{PHL}	Propagation time (propagation delay time) H→L	tPZH	3-state output enable time Z→H
tTLH	Rise time $L \rightarrow H$	tPZL	3-state output enable time Z→L
t _{THL}	Fall time H→L	t _R	Recovery time

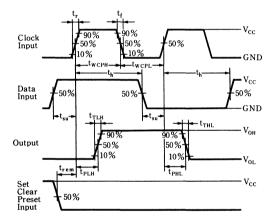


Fig. 11 Set-up time, hold time, propagation time, recovery time, rise time fall time for MN74HC

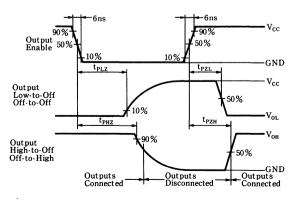


Fig. 12 3-State output propagation time for MN74HC

• Clock rise, fall time (t_r, t_f)

The upper limit of t_r and t_f changes depending on the device and power supply voltage. Unless otherwise specified in the individual data sheet, clock input rise and fall times are less than 6 ns.

● Output rise, fall time (t_{TLH} & t_{THL})

Table 5 t_{TLH} and t_{THL} Characteristics Table (GND=0V, Ta=25°C, t_r , $t_f{\le}6ns$, $C_L{=}50pF$)

Parameter	Symbol	V _{CC} (V)	Min.	Тур.	Max.	Unit
		2.0		25	75	
Output rise time	t _{TLH}	4.5		8	15	ns
		6.0		7	13	
	t _{THL}	2.0		20	75	
Output fall time		4.5		7	15	ns
		6.0		6	13	



5. External Diagrams of Package

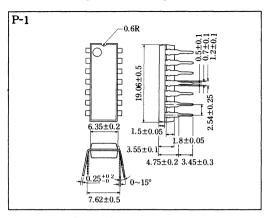


Fig. 13 Plastic DIL-14 pin

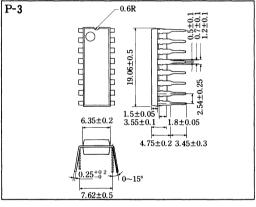


Fig. 15 Plastic DIL-16 pin

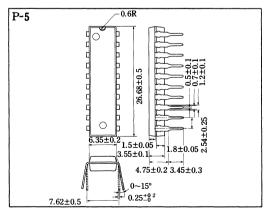


Fig. 17 Plastic DIL-20 pin

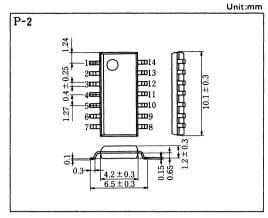


Fig. 14 14-pin Panaflat package (SO-14D)

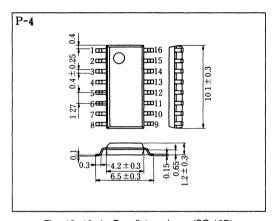


Fig. 16 16-pin Panaflat package (SO-16D)

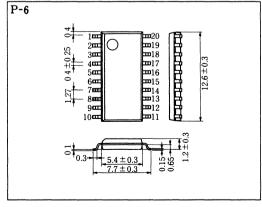


Fig. 18 20-pin Panaflat package (SO-20D)

Individual Specifications



MN74HC00/MN74HC00S

Quad 2-Input NAND Gates

Description

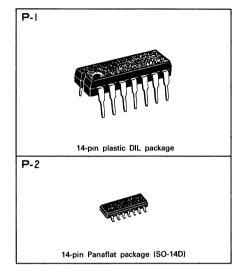
MN74HC00/MN74HC00S contain four 2-input positive isolation NAND gate circuits.

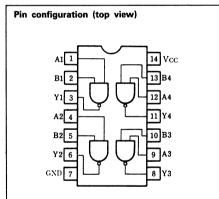
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for the protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit	
Supply volta	ge		Vcc	-0.5∼+7.0	V	
Input/output	t voltage		V_{I}, V_{O}	$-0.5 \sim V_{CC} + 0.5$	V	
Input protec	tion diode current		Iıĸ	±20	mA	
Output paras	sitic diode current		Іок	±20	mA	
Output curre	ent		Io	±25	mA	
Supply curre	ent		I _{CC} , I _{GND}	±50	mA	
Storage tem	perature range		Tstg	-65~+150	°C	
	MNGALICOO	Ta=-40~+60℃	ъ	400	mW	
Power	MN74HC00	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 8mW/°C		
dissipation	141774110000	Ta=-40~+60°C	ъ	275	11/	
	MN74HC00S	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW	



■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t_r, t_f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

	Symbol	V_{CC}	Te	st Condition	ons		•	Femperat	ure		
Parameter		(V)	37	1.		Ta=25 ℃			Ta=-40~+85℃		Unit
			VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		v
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	v
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	V _{OH}	4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		v
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5		20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	II	6.0	$V_I = V_{CC}$	c or GNI)			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	$0,I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

	Symbol	3.7			-	Femperat	ure		Unit
Parameter		V _{cc} (V)	Test Conditions		Ta=25 °ເ	C	Ta=-40)~+85℃	
		(•)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
	t _{THL}	2.0			20	75		95	
Output fall time		4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	tPLH	4.5			8	15		19	ns
(L - 7 11)		6.0			7	13		16	
		2.0			25	75		95	
Propagation time $(H \rightarrow L)$	t _{PHL}	4.5			8	15		19	ns
(II / D)		6.0			7	13		16	

MN74HC02/MN74HC02S

Quad 2-Input NOR Gates

Description

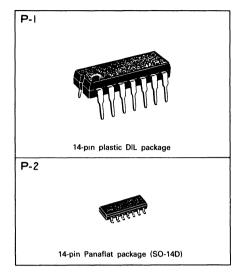
MN74HC02/MN74HC02S contain four 2-input isolation NOR gate circuits.

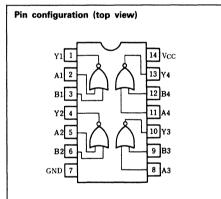
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for the protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

Logic diagram (1 gate)







■ Absolute Maximum Ratings

	Paramete	er	Symbol	Rating	Unit	
Supply volta	ge		V_{CC}	-0.5~+7.0	V	
Input/output	t voltage		V_{I}, V_{O}	$-0.5 \sim V_{CC} + 0.5$	V	
Input protec	ction diode current		Iıĸ	±20	mA	
Output para	sitic diode current		Іок	±20		
Output curre	ent		Io	±25	mA	
Supply curre	ent		I _{CC} , I _{GND}	±50	mA	
Storage tem	perature range		Tstg	-65~+150	c	
	MNZALICOS	Ta=-40~+60°C	D	400	mW	
Power	MN74 HC02	Ta=+60~+85 ℃	P_D	Decrease to 200mW at the rate of 8mW/°C		
dissipation	MNZALICORC	Ta=-40~+60°C	Ъ	275	317	
	MN74HC02S	Ta=+60~+85℃	\mathbf{P}_{D}	Decrease to 200mW at the rate of 3.8mW/°C	mW	



■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~Vcc	V
Operating temperature range	TA		-40~+85	င
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Te	st Conditu	ons		Т	emperatu	ıre		
Parameter	Symbol	V _{CC} (V)	VI	Io		•	Ta=25°	С	Ta=-40)~+85℃	Unit
		(*)	VI	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15		[3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5					ı	0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5		-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	VIL	-20.0	μA	5.9	6.0		5.9		V
		4.5		-4.0	mA	3.86			3.76		
		6.0	l	-5.2	mA	5.36		l	5,26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	v
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA	}		0.32		0.37	
Input current	I_{I}	6.0	$V_I = V_{CC}$	or GNI	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	$D,I_0=0$			2.0		20.0	μΑ

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

		.,							
Parameter	Symbol	V _{CC} (V)	Test Conditions	,	Γa=25℃		Ta=-40	~+85℃	Unit
		(v)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THI} .	4.5			7	15	ĺ	19	ns
		6.0			6	13		16	ns
		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	tPLH	4.5			8	15		19	ns
(2 / 11)		6.0			7	13		16	ns
		2.0			25	75		95	
Propagation time $(H \rightarrow L)$	t _{PHL}	4.5			8	15		19	ns
		6.0			7	13		16	

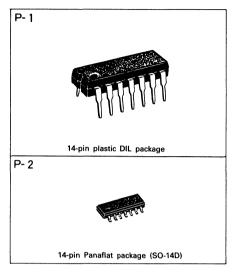
Panasonic -30-

MN74HC03/MN74HC03S

Quad 2-Input NAND Gates (Open Drain)

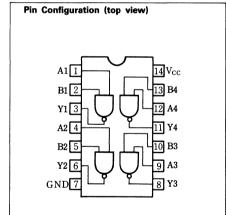
■ Description

MN74HC03/MN74HC03S contain four 2-input open drain positive isolation NAND gate circuits. Input transfer characteristics have been improved by applying a buffer to the gate output, and flutuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND for the protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



■ Logic Diagram (1 gate)





■ Absolute Maximum Ratings

	Parame	ter	Symbol	Rating	Unit			
Supply voltage			V _{cc}	-0.5~+7.0	V			
Input/output voltage			V _I , V _O	-0.5~V _{CC} +0.5	V			
Input protection diode current			I _{IK}	±20	mA			
Output paras	Output parasitic diode current			±20	mA			
Output curre	Output current			t current		Io	±25	mA
Supply curre	Supply current		I _{CC} , I _{GND}	±50	mA			
Storage temp	perature range		Tstg	−65~+150	°C			
	MN74HC03	Ta=-40~+60°C	P _D	400	mW			
Power	WIN74HC03	Ta=+60~+85°C	T r _D	Decrease to 200mW at the rate of 8mW/°C	11144			
dissipation	MN74HC03S	Ta=-40~+60°C	P _D	275	mW			
	WIN /4/1C035	Ta=+60~+85°C	T r _D	Decrease to 200mW at the rate of 3.8mW/°C	11174			



■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input voltage	V _I		0~V _{CC}	v
Output voltage	V _o		*) 0~8.0	V
Operating temperature range	T _A		-40~+85	℃
		V _{CC} =2.0V	0~1000	ns
Input rise and fall time	t _r , t _f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0V	0~400	ns

^{*)} Even if output voltage V_O is less than the absolute maximum rating, Output current I_O might happen to be oven the absolute maximum rating. In this case, pull-up resistance $R(\geqq 390\Omega)$, which is within the absolute maximum rating, is needed to connect with the output pin.

■ DC Characteristics (GND=0V)

		1	Test Conditions								
Parameter	Symbol	V _{CC} (V)	V _I	I _O Unit			Ta=25°C		Ta = -40	Ta=-40~+85°C	
		(,,	VI		Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5	ļ			3.15	į		3.15	İ	V
		6.0	1			4.2]		4.2		v
		2.0						0.3		0.3	v
Input LOW voltage	V_{IL}	4.5						0.9		0.9	v
		6.0					1	1.2		1.2	v
		2.0		20.0	μΑ		0.0	0.1		0.1	V
		4.5	ļ	20.0	μA		0.0	0.1		0.1	v
Output Low voltage	V_{OL}	6.0	V _{IH}	20.0	μΑ		0.0	1.0		0.1	v
		4.5		4.0	mA		ĺ	0.32	1	0.37	v
		6.0		5.2	mA	}		0.32		0.37	v
Input current	I_{I}	6.0	V _I =	V _{CC} or G	ND			±0.1		±1.0	μA
Ouiescent supply current	Icc	6.0	$V_I = V_{CC}$	or GND	$I_0=0$			2.0		20	μA
Output current	I _{OZ}	6.0	V _{IH} , V _{IL} ,	$V_O = V_{CC}$	or GND			±0.5		±5	μΑ

■ AC Characteristics (GND=0V, Input Transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta = -40	~+85°C	Unit
		(, ,		min.	typ.	max.	min.	max.	
	}	2.0			18	75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0			5	13		16	ns
		2.0			13	125		155	
Propagation time (L→Z)	t _{PLZ}	4.5			10	25		31	ns
(2 '2)		6.0			9	21		26	ns
		2.0			14	75		95	
Propagation time (Z←L)	t _{PZL}	4.5		ł	7	15		19	ns
(2 · 2)		6.0			6	13		16	

MN74HC04/MN74HC04S

Hex Inverters

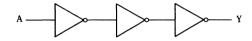
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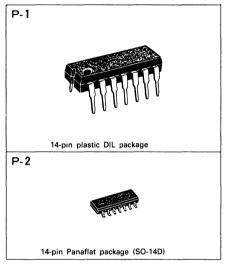
MN74HC04/MN74HC04S contain six inverter circuits.

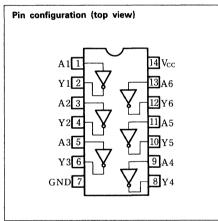
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit		
Supply voltag	ipply voltage		Vcc	-0.5~+7.0	V		
Input/output	ut/output voltage		ut/output voltage		V ₁ , V ₀	$-0.5 \sim V_{CC} + 0.5$	V
Input protection diode current			I _{IK}	±20	mA		
Output parasitic diode current			Іок	±20	mA		
Output current			Io	±25	mA		
Supply current			Icc, Ignd	±50	mA		
Storage temp	ge temperature range		Tstg	-65~+150	C		
	MNZALICOA	Ta=-40~+60°C	ъ	400	117		
MN74HC04 Power		Ta=+60~+85℃	Po	Decrease to 200mW at the rate of 8mW/°C	mW		
dissipation	MN74HC04S	Ta=-40~+60℃	ъ	275	11/		
	MN/4HC045	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	mW		

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~Vcc	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		17	Test	Condition	ıs		Te	mperatu	ire		
Parameter	Symbol	(V)	17			•	Ta=25°	2	Ta=-40	~+85°C	Unit
	,	(•)	Vı	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{II} .	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5		-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	Von	6.0	VIL	-20.0	μ A	5.9	6.0		5.9		V
		4.5		-4.0	mA	3.86	İ		3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5		20.0	μ A		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	ViH	20.0	μ A		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	
,		6.0		5.2	mA			0.32		0.37	
Input current	I_1	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	Icc	6.0	$V_I = V_0$	cc or GNI), $I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

		V_{cc}			Te	mperatu	re		
Parameter	Symbol		Test Conditions	•	Ta=25°)	Ta=-40)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5				15		19	ns
		6.0	,			13		16	
		2.0				75		95	
Output fall time	t _{THI} .	4.5				15		19	n_S
		6.0				13		16	
		2.0				100		125	
Propagation time $(L \rightarrow H)$	t PLH	4.5				20		25	ns
(2 11)		6.0				17		21	
		2.0				100		125	
Propagation time $(H \rightarrow L)$	t PHL	4.5				20		25	ns
(11 / 12)		6.0				17		21	

MN74HCT04/MN74HCT04S

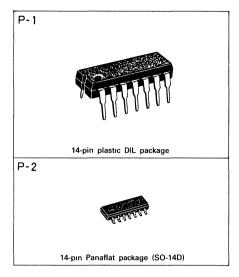
Hex Inverters(TTL Input)

■ Description

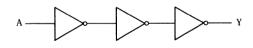
MN74HCT04/MN74HCT04S contain six inverter circuits. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" input and 2.0V or more is logic "1".

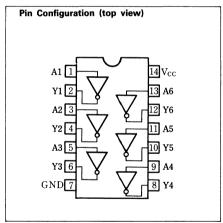
Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



■ Logic Diagram





	Paramet	er	Symbol	Rating	Unit
Supply voltag	ge		V _{CC}	-0.5~+7.0	V
Input/output	voltage		V _I , V _O	-0.5~V _{CC} +0.5	V
Input protect	ion diode current		I_{IK}	±20	mA
Output paras	itic diode current		I _{OK}	±20	mA
Output curre	nt		Io	±25	mA
Supply curren	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	erature range		Tstg	−65~+150	°C
	MN74HCT04	Ta=-40~±60°C	PD	400	mW
Power	WIN74HC 104	Ta=+60~+85°C	I LD	Decrease to 200m Watt the rate of 8mW/°C	111 VV
dissipation	MN74HCT04S	Ta=-40~+60°C	P _D	275	mW
	WII174IIC 1045	Ta=+60~+85°C	r _D	Decrease to 200m Watt the rate of 3.8mW/°C	111 44



Parameter	Symbol	V _{cc} (V)	Rating	Unit
Operation supply voltage	Vcc		4.5~5.5	V
Input/output voltage	V _I , V _O		0∼V _{cc}	V
Operating temperature range	T _A		-40~+85	°C
Input rise and fall time	t _r , t _f	4.5	0~500	ns

■ DC Characteristics (GND=0V)

			Tes	t Conditio	ons		T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	V	ī			Ta=25°C		Ta=-40	~+85°C	Unit
		(,,	Vı	I _O	Unit	min.	typ.	max.	min.	max.	
		4.5				1.5			1.5		V
Input HIGH voltage	V _{IH}	≀				2.0		ĺ	2.0		V
		5.5				4.2			4.2	İ	
		4.5						0.3		0.3	
Input LOW voltage	V_{1L}	. ₹						0.8		0.8	V
		5.5						1.2		1.2	
		4.5		-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}		VIL		·						v
		4.5	l	-4.0	mA	3.86			3.76		
		4.5		20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	V_{OL}		V_{IH}								V
		4.5		4.0	mA			0.32		0.37	
Input current	I _I	5.5	V _I =	V _{CC} or G	ND			±0.1		±1.0	μΑ
Quiescent supply current	I_{CC}	5.5	$V_I = V_{CC}$	or GND	$I_{O}=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transistion time \leq 6ns, C_L=50pF)

					T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta = -40	~+85°C	Unit
		(, ,		min.	typ.	max.	min.	max.	
Output rise time	t _{TLH}	4.5			4	15		19	ns
Output fall time	t _{THL}	4.5			4	15		19	ns
Propagation time $(L \leftarrow H)$	t _{PLH}	4.5			7	20		25	ns
Propagation time (H←L)	t _{PHL}	4.5			6	20		25	ns

MN74HCU04/MN74HCU04S

Hex Inverters (Unbuffered)

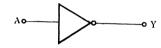
■ Description

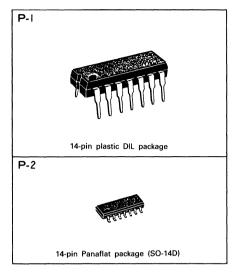
MN74HC04/MN74HC04S contain six inverter circuits without buffer.

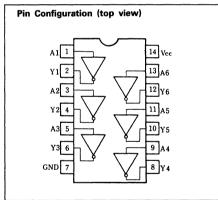
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







	Paramete	r	Symbol	Rating	Unit
Supply volta	ge		Vcc	-0.5~+7.0	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protec	tion diode current		I _{IK}	±20	mA
Output paras	sitic diode current		Іок	±20	mA
Output curre	ent		Io	±25	mA
Supply curre	ent		I _{CC} , I _{GND}	±50	mA
Storage tem	perature range		Tstg	-65~+150	င
	MN74 HCU04	Ta=-40~+60℃	P_{D}	400	mW
Power	MIN74 HCUU4	Ta=+60~+85 ℃	r _D	Decrease to 200mW at the rate of 8mW/°C	m vv
dissipation	MN74 HCU04 S	Ta=-40~+60°C	D.	275	mW
	MN74HCUU4S	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	m vv



Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Tes	st Conditio	ns		Te	emperatu	re	Ī	
Parameter	Symbol	V _{CC} (V)	V	,			Ta=25°	C	Ta=-40	~+85°C	Unit
		(*)	Vı	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.7			1.7		
Input HIGH voltage	V_{IH}	4.5				3.6		}	3.6		V
		6.0				4.8			4.8		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.8		0.8	v
		6.0						1.1		1.1	
		2.0		-20.0	μA	1.8	2.0		1.8		
		4.5		-20.0	μA	4.0	4.5		4.0		
Output HIGH voltage	V_{OH}	6.0	VIL	-20.0	μ A	5.5	6.0		5.5		v
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.2		0.2	
		4.5	}	20.0	μΑ		0.0	0.5]	0.5	
Output LOW voltage	V_{OL}	6.0	VIH	20.0	μΑ		0.0	0.5		0.5	V
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32	1	0.37	
Input current	I_{I}	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	$0,I_0=0$			2.0		20.0	μA

\blacksquare AC Characteristics (GND=0V, Input transition time ${\leq}6\text{ns},~C_L{=}50\text{pF})$

		3.7			T	emperatu	ire		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°	C	Ta=-40	~+85℃	Unit
		(''		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	tTHL	4.5		ļ	7	15		19	ns
		6.0			6	13		16	
		2.0			20	75		95	
Propagation time $(L \rightarrow H)$	tPLH	4.5			6	15		19	ns
, , , , ,		6.0			5	13		16	
		2.0			20	75		95	
Propagation time $(H \rightarrow L)$	tPHL	4.5			6	15		19	ns
(41 / 22)		6.0			5	13		16	

MN74HC08/MN74HC08S

Quad 2-Input AND Gates

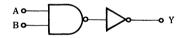
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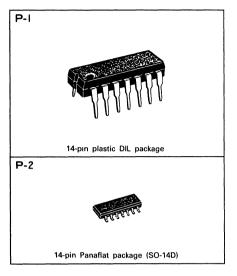
MN74HC08/MN74HC08S contain four 2-input positive isolation AND gate circuits.

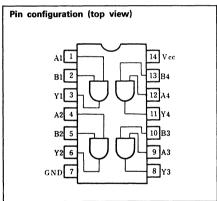
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







	Parameter			Rating	Unit				
Supply volta	y voltage		y voltage		y voltage		Vcc	$-0.5 \sim +7.0$	V
Input/output	voltage		V_{I}, V_{O}	$-0.5 \sim V_{\rm cc} + 0.5$	V				
Input protec	tion diode current		I _{IK}	±20	mA				
Output paras	sitic diode current		Іок	±20	mA				
Output curre	ent		Io	±25	mA				
Supply curre	ent		I _{CC} , I _{GND}	±50	mA				
Storage tem	perature range		Tstg	−65∼+150	C				
	MN74 HC08	Ta=-40~+60°C	D	400	117				
Power $Ta=+60\sim+85$ °C		P_D	Decrease to 200mW at the rate of 8mW/°C	mW					
dissipation			n	275					
	MN74HC08S		P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW				



Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_{I},V_{O}		0~V _{CC}	V
Operating temperature range	TA		−40∼+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Те	st Condition	ons		To	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vı	Io			Ta=25°	С	Ta=-40)~+85℃	Unit
		(•)	VI	71 10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3,15)		3.15		v
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	v
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5		-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	VIH	-20.0	μA	5.9	6.0		5.9		v
		4.5		-4.0	mૃΑ	3.86			3.76	1	
		6.0		-5.2	mA	5.36			5.26]	
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	v
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	II	6.0	$V_I = V_C$	c or GNI)			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	$D,I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

					Te	emperatu	re		
Parameter	Symbol	Vcc	Test Conditions		Ta=25°		Ta=-40)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	tTHL	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	tPLH	4.5			8	15		19	ns
(L → 11)		6.0			7	13		16	
		2.0			25	75		95	
Propagation time $(H \rightarrow L)$	tPHL	4.5			8	15		19	ns
(II → L)		6.0			7	13		16	

MN74HC10/MN74HC10S

Triple 3-Input NAND Gates

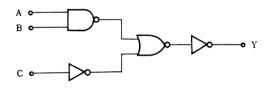
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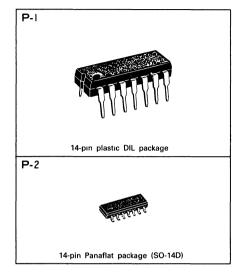
MN74HC10/MN74HC10S contain three 3-input positive isolation AND gate circuits.

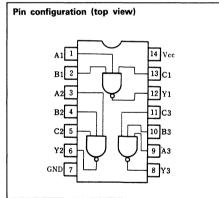
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







	Paramete	er	Symbol	Rating	Unit			
Supply volta	Supply voltage			y voltage		Vcc	-0.5~+7.0	V
Input/output	t/output voltage		V_{I},V_{O}	$-0.5 \sim V_{\rm CC} + 0.5$	V			
Input protec	tion diode current		I _{IK}	±20	mA			
Output paras	sitic diode current		Іок	±20	mA			
Output current			Ιo	±25	mA			
Supply curre	ent		$I_{CC,I_{GND}}$	±50	mA			
Storage tem	perature range		Tstg	-65~+150	°C			
	M N74HC10	Ta=-40~+60℃	n	400	mW			
Power $Ta=+60\sim+85$ °C		P_D	Decrease to 200mW at the rate of 8mW/°C	m w				
dissipation			ъ	275	117			
MN74HC10S $T_a = +60 \sim +85 \text{°C}$			P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW			



Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_{I}, V_{O}		$0 \sim V_{\rm CC}$	V
Operating temperature range	TA		-40~+85	ဗ
		2.0	0~1000	ns
Input rise and fall time	t_r, t_f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Te	st Condition	ons		T	emperatu	re		
Parameter	Symbol	V_{CC} (V)	Vı	_		,	Γa=25°	c	Ta=-40	0~+85℃	Unit
		(v)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		v
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	v
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		v
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5		20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	VIH	20.0	μA		0.0	0.1		0.1	V
_		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	II	6.0	$V_{I}=V_{C}$	or GNI)			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_1 = V_{C}$	c or GN	$D,I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

					T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Ta=25°	2	Ta=-40)~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	tPLH	4.5			8	15		19	ns
$(L \rightarrow \Pi)$		6.0			7	13		16	
		2.0			25	75		95	
Propagation time $(H \rightarrow L)$	tPHL	4.5			8	15		19	ns
	-, 1112	6.0			7	13		16	

MN74HC11/MN74HC11S

Triple 3-Input AND Gates

■ Description

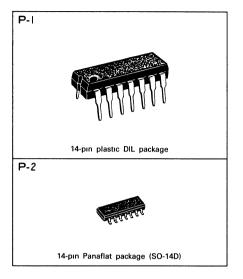
MN74HC11/MN74HC11S contain three 3-input positive isolation AND gate circuits.

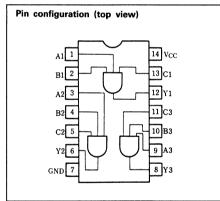
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic Diagram







Parameter			Symbol	Rating	Unit
Supply voltage	ge		V _{CC}	-0.5~+7.0	V
Input/output	voltage		V_{I}, V_{O}	$-0.5 \sim V_{\rm cc} + 0.5$	V
Input protect	Input protection diode current			±20	mA
Output parasitic diode current			Іок	±20	mA
Output current			Io	±25	mA
Supply curre	ent		I _{CC} , I _{GND}	±50	mA
Storage temp	perature range		Tstg	-65~+150	$^{\circ}$
	MN74 HC11	Ta=-40~+60°C	D	400	117
Power Ta=+60~+85℃		P_D	Decrease to 200mW at the rate of 8mW/°C	mW	
dissipation	1 1a=-40~+60(:		ъ	275	117
MN74HC11S $T_a = +60 \sim +85 ^{\circ}$			P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_{I}, V_{O}		$0 \sim V_{\rm CC}$	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t_r, t_f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		.,,	Tes	st Condition	ons		Te	st Condit	ions		
Parameter	Symbol	(V)	Vı	Io			Ta=25°	C	Ta=-4	0~+85℃	Unit
		(, ,	V1	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5		-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	V_{IH}	-20.0	μA	5.9	6.0		5.9		V
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Ii	6.0	$V_I = V_{CC}$	c or GNI)			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	$D,I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

		V_{CC}			Т	est Condi	tions		
Parameter '	Symbol	(V)	Test Conditions	,	Ta=25°		Ta=-40)~+85℃	Unit
		(, ,		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	tTHL	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	tplh	4.5			8	15		19	ns
(L → II)		6.0			7	13		16	
		2.0			25	75		95	
Propagation time (H → L)	tPHL	4.5			8	15		19	ns
(II , D)		6.0			7	13		16	

MN74HC14/MN74HC14S

Hex Inverting Schmitt Triggers

■ Description

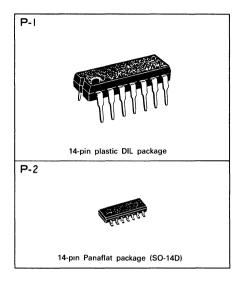
MN74HC14/MN74HC14S contains six inverter circuits with Schmitt triggers at all input terminals.

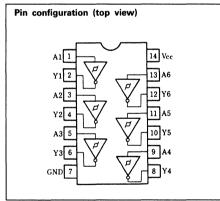
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Because the circuit threshold voltage differs $(V_{IH} \ V_{IL})$ when the input waveform rises and falls, wider applications are possible for the line receiver, waveform shaping and multi-vibrator in addition to the normal inverter.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

■ Logic Diagram (1 Gate)







Parameter			Symbol	Rating	Unit		
Supply voltag	ply voltage		Vcc	-0.5~+7.0	V		
Input/output	tput voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V		
Input protection diode current			Iıĸ	±20	mA		
Output paras	sitic diode current		Іок	±20	mA		
Output current			Io	±25	mA		
Supply curre	nt		$I_{CC,}I_{GND}$	±50	mA		
Storage tem	perature range		Tstg	−65∼+150	C		
	Ta=-40~+60℃		Ta=-40~+60°C		D	400	117
Power MN74 HC14 $T_a = +60 \sim +85 ^{\circ}\text{C}$		$\mathbf{P}_{\mathtt{D}}$	Decrease to 200mW at the rate of 8mW/°C	mW			
dissipation	dissipation $Ta = -40 \sim +60 \degree$		Ъ	275	117		
MN74HC14S $T_a = +60 \sim +85 \%$			P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW		

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V ₁ , V ₀		0 ~ V _{CC}	V
Operating temperature range	TA		-40~+85	c

■ DC Characteristics (GND=0V)

		V_{CC}	Tes	st Condition	ons		T	emperatu	re		
Parameter	Symbol	(V)	VI	Io			Ta=25 °	2	Ta=-40	~+85 ℃	Unit
			VI	V1 10	Unit	min.	typ.	max.	min.	max.	
	$ m V_{OH}$	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5	j	4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0	Ì	5.9		V
		4.5	V _{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_I = V_C$	or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_1 = V_C$	c or GN	$D,I_0=0$			2.0		20.0	μA
		2. 0				0.7	1.10	1.50	0.7	1.5	
	V_T +	4.5				1.55	2.46	3.15	1.55	3.15	V
Input threshold voltage		6.0	ļ			2.1	3. 25	4.2	2.1	4.2	
		2.0	İ			0.3	0.80	1.0	0.3	1.0	
	V _T -	4.5				0.9	2.00	2.45	0.9	2.45	V
		6.0				1.2	2.60	3.2	1.2	3.2	
TT		2.0				0.2	0.3	1.2	0.2	1.2	
Hysteresis voltage	V _H	4.5				0.4	0.5	2.1	0.4	2.1	V
		6.0				0.5	0.7	2.5	0.5	2.5	

\blacksquare AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

		Vcc			Te	mperatur	e		
Parameter	Symbol	(V)	Test Conditions		Ta=25 °C		Ta=-40)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
D (1)		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	tPLH	4.5			8	15	İ	19	ns
		6.0			7	13	Ì	16	
Propagation time $(H \rightarrow L)$		2.0			25	75		95	
	t _{PHL}	4.5			8	15		19	ns
		6.0			7	13		16	

MN74HC20/MN74HC20S

Dual 4-Input NAND Gates

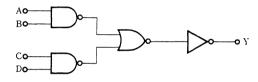
■ Description

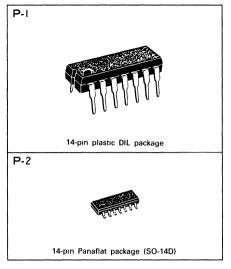
MN74HC20/MN74HC205 contain two 4-input positive isolation NAND gate circuits.

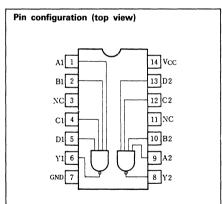
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







	Paramete	er	Symbol	Rating	Unit
Supply voltage			Vcc	-0.5~+7.0	V
Input/output	ut/output voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	v
Input protec	tion diode current		I _{IK}	±20	mA
Output paras	sitic diode current		Іок	±20	mA
Output curre	Output current			±25	mA
Supply curre	ent		I_{CC}, I_{GND}	±50	mA
Storage tem	perature range		Tstg	-65∼+150	°C
	MNZALICOO	Ta=-40~+60°C	P_{D}	400	mW
Power	Power $MN74 HC20$ $Ta=+60\sim+85^{\circ}$			Decrease to 200mW at the rate of 8mW/°C	m vv
dissipation	dissipation $MN74HC20S$ $Ta=-40\sim+60^{\circ}$		ъ	275	137
$Ta = +60 \sim +85^{\circ}$			$\mathbf{P}_{\mathtt{D}}$	Decrease to 200mW at the rate of 3.8mW/°C	mW

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	v
Input/output voltage	V _I , V _O		$0 \sim V_{\rm CC}$	v
Operating temperature range	Т		-40~+85	င
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Те	st Condition	ons		T	emperat	ure		
Parameter	Symbol	V _{CC} (V)	Vı			Ta=25℃			Ta=-40)~+85℃	Unit
		()	νı	V _I I _O	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	v
-		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		v
		4.5	VIL	-4.0	mA	3.86		Ì	3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5		20.0	μA		0.0	0.1	[0.1	
Output LOW voltage	Vol	6.0	VIH	20.0	μA		0.0	0.1		0.1	V
Output EOW Voltage		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or GN	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GNI	$D,I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

		V_{CC}			Te	mperatur	·e		
Parameter	Symbol	(V)	Test Conditions		Ta=25°	2	Ta=-40)~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
_		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	tPLH	4.5			8	15		19	ns
(=)		6.0			7	13		16	
Propagation time $(H \rightarrow L)$		2.0			25	75		95	
	tPHL	4.5			8	15		19	ns
		6.0			7	13		16	

MN74HC21/MN74HC21S

Dual 4-Input AND Gates

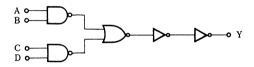
■ Description

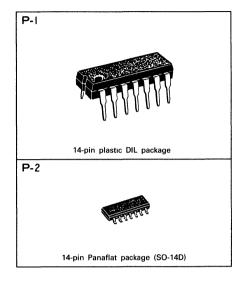
MN74HC21/MN74HC21S contain two 4-input positive isolation AND gate circuits.

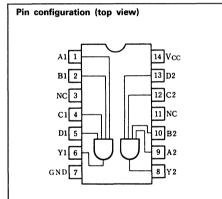
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







	Paramet	er	Symbol	Rating	Unit
Supply volta	ge		Vcc	-0.5~+7.0	v
Input/output	voltage		V _I , V _o	$-0.5 \sim V_{\rm cc} + 0.5$	V
Input protec	tion diode current		Iık	±20	mA
Output para	sitic diode current		Iok	±20	mA
Output current			Io	±25	mA
Supply curre	ent		I _{CC} ,I _{GND}	±50	mA
Storage tem	perature range		Tstg	-65∼+150	${\mathfrak C}$
	MN74 HC91	Ta=-40~+60℃	D	400	mW
Power $MN74 HC21$ $T_a = +60 \sim +85^{\circ}$			P_D	Decrease to 200mW at the rate of 8mW/°C	mvv
dissipation			D	275	mW
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$			$\mathbf{P}_{\mathtt{D}}$	Decrease to 200mW at the rate of 3.8mW/°C	m vv

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	$V_{\rm I}, V_{\rm O}$		$0 \sim V_{\rm CC}$	v
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		W	Те	st Conditi	ons		Т	emperati	ıre		
Parameter	Symbol	Vcc					Ta=25°	C	Ta=-40	~+85℃	Unit
		(V)	Vi	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5		1				0.9		0.9	V
		6.0						1.2		1.2	
	V _{он}	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5		-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	VIH	-20.0	μA	5.9	6.0		5.9		V
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
a super a survey		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	$I_{\rm I}$	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	D,Io=0			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

		V_{cc}			Te	emperatu	re		
Parameter	Symbol	(V)	Test Conditions:	·	Ta=25°		Ta=-40)~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	t _{PLH}	4.5			8	15		19	ns
(L→11)		6.0			7	13		16	
Propagation time $(H \rightarrow L)$		2.0			25	75		95	
	tPHL	4.5			8	15		19	ns
		6.0			7	13		16	

MN74HC27/MN74HC27S

Triple 3-Input NOR Gates

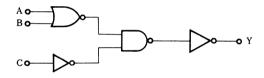
■ Description

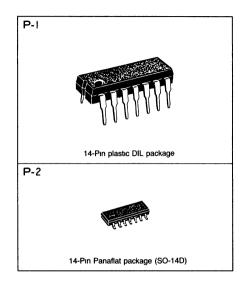
MN74HC27/MN74HC27S contain three 3-input positive isolation NOR gate circuits.

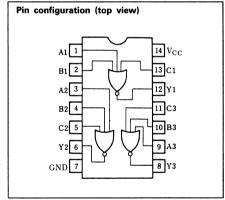
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







	Paramete	r	Symbol	Rating	Unit		
Supply volta	ige		Vcc	-0.5~+7.0	V		
Input/outpu	out voltage		itput voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protec	ction diode current		Iıĸ	±20	mA		
Output para	sitic diode current		Iok	±20	mA		
Output curr	Output current			±25	mA		
Supply curre	ent		I _{CC} , I _{GND}	±50	mA		
Storage tem	perature range		Tstg	−65~+150	${\mathfrak C}$		
	MN74 HC27	Ta=-40~+60°C	P_{D}	400	mW		
Power	T 100 105%			Decrease to 200mW at the rate of 8mW/°C	m vv		
dissipation	dissipation MN74HC27S $Ta = -40 \sim +60 ^{\circ}$			275	mW		
	$Ta = +60 \sim +85^{\circ}$			Decrease to 200mW at the rate of 3.8mW/°C	m vv		



Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	v
Input/output voltage	V _I ,V _O		0~Vcc	v
Operating temperature range	TA		-40~+85	င
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Te	st Condition	ons		Т	emperati	ıre		
Parameter	Symbol	Vcc	W			•	Γa=25°	C	Ta=-40	~+85℃	Unit
		(V)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	V _{OH}	4.5		-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	VIL	-20.0	μA	5.9	6.0		5.9		V
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	V _I =V _{CC} or GND				±0.1		±1.0	μA	
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	$D,I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

		3.7			Te	emperatu	re		
Parameter	Symbol	V _{CC}	Test Conditions	,	Ta=25℃	2	Ta=-40)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
-		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	tPLH	4.5			8	15		19	ns
(= ',		6.0			7	13		16	
		2.0			25	75		95	
Propagation time $(H \rightarrow L)$	t _{PHL}	4.5			8	15		19	ns
		6.0			7	13		16	

MN74HC30/MN74HC30S

8-Input NAND Gates

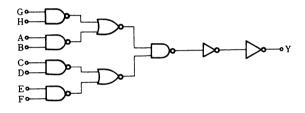
■ Description

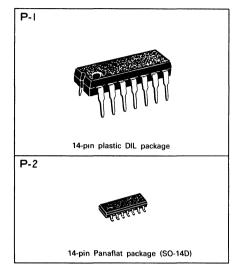
MN74HC30/MN74HC30S contain one 8-input positive isolation NAND gate circuits.

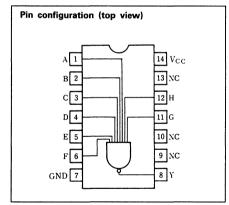
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







	Paramete	r	Symbol	Rating	Unit						
Supply voltage	ge		Vcc	-0.5~+7.0	V						
Input/output	voltage		voltage		voltage		voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	v
Input protect	tion diode current		Iıĸ	±20	mA						
Output paras	sitic diode current		Ioĸ	±20	mA						
Output curre	ent		Io	±25	mA						
Supply curre	ent		I _{CC} , I _{GND}	±50	mA						
Storage tem	perature range		Tstg	−65~+150	${\mathbb C}$						
	MN74 HC30	Ta=-40~+60°C	ъ	400	mW						
Power $Ta=+60$		Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 8mW/°C	m vv						
dissipation	MNZALICZOC	Ta=-40~+60°C	ъ	275							
	MN74HC30S	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW						



Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	v
Input/output voltage	V _I ,V _O		$0 \sim V_{\rm cc}$	v
Operating temperature range	TA		-40~+85	°
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Tes	st Conditio	ns			Tempera	ature		
Parameter	Symbol	V _{CC} (V)	17	,		,	Ta=25°	С	Ta=-40	~+85°C	Unit
		(•)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μA	5.9	6.0	1	5.9		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5		20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	V _{IH}	20.0	μA		0.0	0.1		0.1	V
, , , , , , , , , , , , , , , , , , , ,		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V_C$	V _I =V _{CC} or GND				±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	$D,I_0=0$			2.0		20.0	μΑ

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

		V_{CC}			Т	emperatı	ıre		
Parameter	Symbol	(V)	Test Conditions		Ta=25℃		Ta=-40)~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			43	150		190	
Propagation time $(L \rightarrow H)$	tPLH	4.5			16	30		38	ns
		6.0			12	26		33	
		2.0			35	125		155	
Propagation time $(H \rightarrow L)$	tPHL	4.5			14	25		31	ns
		6.0			7	21		26	

MN74HC32/MN74HC32S

Quad 2-Input OR Gates

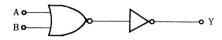
■ Description

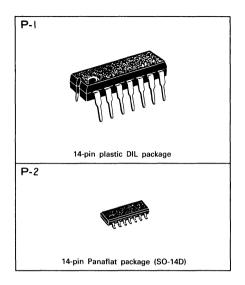
MN74HC32/MN74HC32S contain four 2-input positive isolation OR gate circuits.

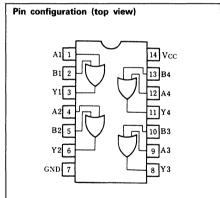
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)







	Paramete	er	Symbol	Rating	Unit
Supply voltage	ge		Vcc	-0.5~+7.0	V
Input/output	ut voltage		V_{I}, V_{O}	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protect	tion diode current		Ιικ	±20	mA
Output paras	sitic diode current		Iok	±20	mA
Output curre	ent		Io	±25	mA
Supply curre	ent		I _{CC} , I _{GND}	±50	mA
Storage tem	perature range		Tstg	-65~+150	C
	MN74 HC32	Ta=-40~+60℃	ъ	400	117
Power $Ta=+60\sim+85$		Ta=+60~+85 ℃	P_D	Decrease to 200mW at the rate of 8mW/°C	mW
dissipation	MNZALICAGE	Ta=-40~+60℃	D	275	. 387
	MN74HC32S	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_{I}, V_{O}		$0 \sim V_{\rm CC}$	v
Operating temperature range	TA		-40~+85	င
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
	,	6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Tes	st Conditio	ons		7	emperat	ure		
Parameter	Symbol	V _{cc} (V)	Vı	_		•	Ta=25°	C	Ta=-40	~+85℃	Unit
		(*/	VI	Io	Unit Unit		typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5	İ					0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	Voh	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5		20.0	μA		0.0	0.1	ĺ	0.1	
Output LOW voltage	V_{OL}	6.0	VIL	20.0	μΑ		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	V _I =V _{CC} or GND				±0.1		±1.0	μA	
Quiescent supply current	I_{cc}	6.0	$V_{I} = V_{C}$	or GNI	$0,I_0=0$			2.0		20.0	μA

\blacksquare AC Characteristics (GND=0V, Input transition time ${\leq}6ns,~C_L{=}50pF)$

		V_{CC}			7	[emperat	ure		
Parameter	Symbol	V CC (V)	Test Conditions	,	Ta=25 °C		Ta=-40	~+85℃	Unit
				min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7.	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			25	75		95	
Propagation time $(L \rightarrow H)$	tPLH	4.5			8	15		19	ns
(=/		6.0			7	13		16	
Propagation time $(H \rightarrow L)$		2.0			25	75		95	
	t _{PHL}	4.5			8	15		19	ns
		6.0			7	13		16	

MN74HC42/MN74HC42S

BCD-to-Decimal Decoder

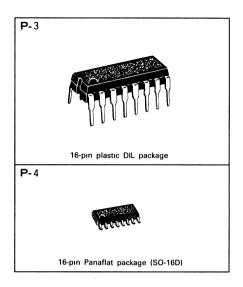
■ Description

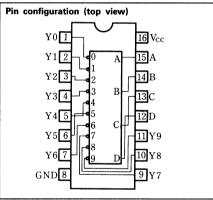
MN74HC42/MN74HC42S are BCD-to-Decimal Decorder. Only outputs from 10 outputs ($Y0\sim Y9$) corresponding to inputs ($A\sim D$) become "L". All other outputs become "H". When input becomes over 9, all outputs become "H".

Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent ot CMOS, and an operation speed of LS TTL. Each output can directly drive LS TTL 10-inputs. A Resistors and diode are provided between the $V_{\rm CC}$ and GND to protect the input and output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

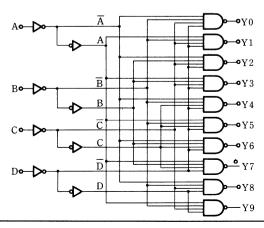
■ Truth table

A.T		Inp	out						Out	put				
No.	D	С	В	Α	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
1	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
2	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
3	L	L	Н	Н	Ή	Н	Н	L	Н	Н	Н	Н	Н	Н
4	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
5	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
6	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
7	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
8	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
9	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
Ħ	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
utp	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
)e 0	Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Ineffective output	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
effe	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
드	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н





■ Logic Diagram





■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit
Supply voltage	ge	, , , , , , , , , , , , , , , , , , ,	$V_{\rm CC}$	-0.5~+7.0	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm cc} + 0.5$	v
Input protect	ion diode current		I _{IK}	±20	mA
Output paras	itic diode current		Іок	±20	mA
Output curre	ent	i		±25	mA
Supply curre	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	perature range		Tstg	-65~+150	°C
	MN74HC42	Ta=-40~+60℃	P_{D}	400	mW
Power	Ta=+60~+85°C		ΓĐ	Decrease to 200mW at the rate of 8mW/°C	111 VV
dissipation	MN74HC42S	Ta=-40~+60°C	P_{D}	275	mW
	MN/471C425	Ta=+60~+85℃	PD	Decrease to 200mW at the rate of 3.8mW/°C	m vv

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V_{I}, V_{O}		0~V _{cc}	v
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

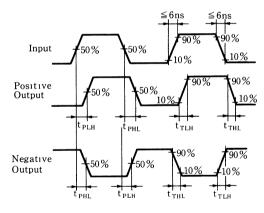
■ DC Characteristics (GND=0V)

= PO GIIGI GOLOGO	10115	•,									
		.,	Tes	st Conditio	ons		T	emperatu	ire		
Parameter	Symbol	V _{CC}	٠,,	_		•	Ta=25℃		Ta=-40)~+85℃	Unit
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Io	Unit	min.	typ.	max.	min.	max.				
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0	1	5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	$D, I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

					Tei	nperatu	re		
Parameter	Symbol	V _{CC} (V)	'Test Conditions	Ta=25℃			Ta = -40	~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0			26	75		95	
Output rise time	tTLH	4.5			11	15		19	ns
		6.0			8	13		16	
		2.0			21	75		95	
Output fall time	t _{THL}	4.5			8	15		19	ns
		6.0			6	13		16	
D		2.0			39	125		155	
Propagation time $A, B, C, D \rightarrow Y (L \rightarrow H)$	t _{PLH}	4.5			18	25		31	ns
$A, B, C, D \rightarrow I (L \rightarrow H)$		6.0			13	21		26	
D		2.0			36	125		155	
Propagation time	t PHL	4.5			15	25		31	ns
$A,B,C,D\rightarrow Y (H\rightarrow L)$		6.0			11	21		26	

■ AC Characteristics Measuring Waveforms



MN74HC51/MN74HC51S

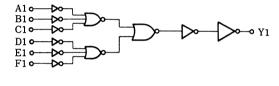
Dual AND-OR Invert Gates

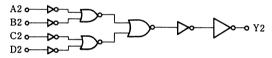
■ Description

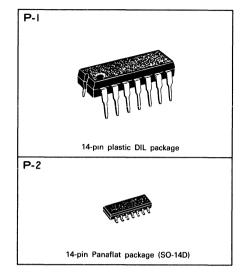
MN74HC51/MN74HC51S contain two AND-OR-INVERT gates. Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

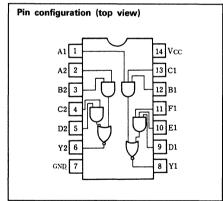
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic diagram (1 gate)









	Paramete	er	Symbol	Rating	Unit	
Supply volta	ge		Vcc	-0.5~+7.0	V	
Input/output	voltage		V_{I}, V_{O}	$-0.5 \sim V_{\rm CC} + 0.5$	V	
Input protec	t protection diode current			±20	mA	
Output para	sitic diode current		Iok	±20	mA	
Output curre	ent		Io	±25	mA	
Supply curre	ent			±50	mA	
Storage tem	perature range		Tstg	−65∼+150	$^{\circ}$	
	MN74HC51	Ta=-40~+60°C	ъ	400	mW	
Power	MN74HC51	Ta=+60~+85°C	P_D	Decrease to 200mW at the rate of 8mW/°C	m vv	
dissipation	MN74HC51S	Ta=-40~+60°C	ъ	275	337	
	MIN/4HC51S	Ta=+60~+85°C	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	mW	

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	v
Input/output voltage	V _I , V _O		0~V _{cc}	v
Operating temperature range	T _A		-40~+8 5	r
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

= DO GHAIACTERISTICS	, , , , , , ,	-,	,								
		3.7	Те	st Condition	ons		T	emperatu	ire		
Parameter	Symbol	V _{CC} (V)	VI	,		•	Γa=25°	C	Ta=-40	~+85℃	Unit
		(*)	V1	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	$\mathbf{I}_{\mathbf{I}}$	6.0	$V_I = V_C$	c or GNI)			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_{\rm I} = V_{\rm C}$	c or GNI	$I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

					T	emperatu	ire		
Parameter	Symbol	Vcc	Test Conditions		Ta=25℃	2	Ta=-40	~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
_		2.0			40	150		190	
Propagation time $(L \rightarrow H)$	tPLH	4.5		İ	16	30		38	ns
(2 11)		6.0			11	26		33	
_		2.0			39	125		155	
Propagation time $(H \rightarrow L)$	t _{PHL}	4.5			13	25		31	ns
(<u>-</u> /		6.0			10	21		26	

MN74HC73/MN74HC73S

Dual J-K Flip-Flops with Clear

■ Description

MN74HC73/MN74HC73S contain two J-K flip-flop circuits with clear. Each flip-flop has independent clear, J-K, clock input and complementary Q and \overline{Q} outputs. Input data is transferred to the output on the negative going edge of the clock pulse. Clear operates at LOW level regardless of the clock. Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to CMOS, and an operation speed of LS TTL. Each output can directly drive LS TTL 10-inputs.

Resistors and diode are provided between the $V_{\rm CC}$ GND to protect the input and output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Truth Table

	Inp	Ou	Output		
CLR	CLK	J	K	Q	$\overline{\overline{\mathbf{Q}}}$
L	×	×	×	L	Н
Н	٦.	L	L	Q0	$\overline{\overline{\mathbf{Q}}}0$
Н	٦.	Н	L	Н	L
Н	Z	L	Н	L	Н
Н	Z	Н	Н	Tog	gle
Н	Н	×	×	Q0	$\overline{\overline{\mathbf{Q}}}0$

Note:

1. ×: Either HIGH or LOW; it doesn't matter

2. \(\frac{1}{2}\): Rise of negative direction

3. \vec{Q}_{O} : Q level prior to determination of input condition shown in

4. \overline{Q}_0 : Q level prior to determination of input condition shown in

5. Toggle: With → change, output becomes a complement of the previous condition

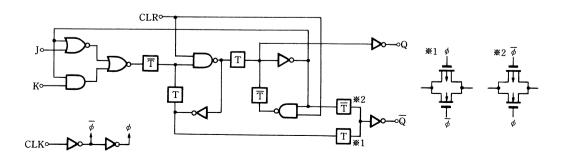
CLR 2

10 K2

9 Q2

P-1

■ Logic diagram (1 gate)



■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit
Supply voltag	ge		$V_{\rm cc}$	-0.5~+7.0	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protect	tion diode current		I _{IK}	±20	mA
Output paras	sitic diode current		Іок	±20	mA
Output curre	Output current			±25	mA
Supply curre	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	perature range		Tstg	-65~+150	C
	MN74HC73	Ta=-40~+60°C	P_{D}	400	mW
Power	T160 105°C			Decrease to 200mW at the rate of 8mW/°C	m vv
dissipation	MN74HC73S	Ta=-40~+60℃	D.	275	mW
	MN/4HC/35	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	III VV

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t_r, t_f	4.5	0~500	ns
		6.0	0~400	ns

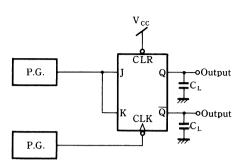
■ DC Characteristics (GND=0V)

		17	Te	st Condition	ons		7	emperat	ure		
Parameter	Symbol	V _{cc} (V)	Vı	,		,	Γa=25°		Ta=-40)~+85℃	Unit
		(v)	V 1	V _I I _O	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0	1	5.9		V
		4.5	V_{IL}	-4.0	mA	3.86		1	3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1	!	0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	II	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_1 = V_C$	c or GNI	D, I ₀ =0			4.0		40.0	μA

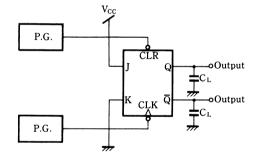
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

Parameter			Test Conditions	Temperature						
	Symbol	Vcc			Ta=25°	С	Ta=-40	Unit		
		(V)		min.	typ.	max.	min.	max.		
		2.0				75		95		
Output rise time	tTLH	4.5			8	15		19	ns	
		6.0				13		16		
		2.0				75		95		
Output fall time	t _{THL}	4.5			6	15		19	ns	
		6.0				13		16		
D		2.0				125		155		
Propagation time	tplh	4.5			15	25		31	ns	
$CLK \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0				21		26		
Duna antina star		2.0				125		155		
Propagation time	t _{PHL}	4.5			13	25		31	ns	
$CLK \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0				21		26		
D		2.0				175		220		
Propagation time	t _{PLH}	4.5			22	35		44	ns	
$CLR \rightarrow \overline{Q} (L \rightarrow H)$		6.0				30		37		
D		2.0				150		190		
Propagation time	t _{PHL}	4.5			17	30		38	ns	
CLR→Q (H→L)		6.0				26		33		
3.6.		2.0				75		95		
Minimum pulse width	tw	4.5			7	15		19	ns	
CLR		6.0				13		16		
		2.0				100		125		
Minimum Set-up time	t_{su}	4.5			6	20		25	ns	
		6.0				17		21		
		2.0			_	0		0		
Minimum Hold time	th	4.5				0		0	ns	
		6.0			_	0		0		
Minimum recovery time		2.0				75		95		
	trem	4.5			2	15		19	ns	
		6.0				13		16		
		2.0		6			4			
Maximum clock frequency	f max.	4.5		30	72		24		MHz	
,		6.0		35			28			

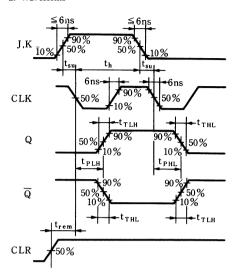
- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , t_{su} , t_{max} , t_{PLH}/t_{PHL} (CLKightarrow Q, \overline{Q}), t_{rem} , t_h
 - 1. Measuring Circuit (t_{PLH},t_{PHL})



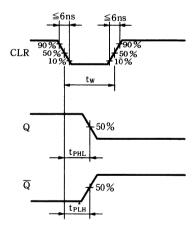
[2] t_{PLH}/t_{PHL} (CLR→Q, Q), t_W
 1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



2. Waveforms



MN74HC74/MN74HC74S

Dual D-Type Flip-Flops with Preset and Clear

■ Description

MN74HC74/MN74HC74S contain two D-type flip-flop circuits with preset and clear. Each flip-flop has independent clear, preset, data, clock input and complementary Q and \overline{Q} outputs. Input data is transferred to the output on the positive going edge of the clock pulse. Preset and clear operate at LOW level regardless of the clock. Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to CMOS, and an operation speed of LS TTL. Each output can directly drive LS TTL 10-inputs.

Resistors and diodes are provided between the $V_{\rm CC}$ GND to protect of the input and output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Truth table

	Inp	Outp	Output			
PR	CLR	CLK	D	Q	\overline{Q}	
L	Н	×	×	Н	L	
Н	L	×	×	L	Н	
L	L	×	×	H*	Н*	
Н	Н	<u> </u>	Н	Н	L	
Н	Н	5	L	L	Н	
Н	Н	L	×	Q_0	$\overline{\overline{\mathbf{Q}}}_{0}$	

No	te:
1.	×:

Either HIGH or LOW; it doesn't matter

2. \mathcal{J} : Rise of positive direction

3. Q_o: Q level prior to determination of input condition shown in

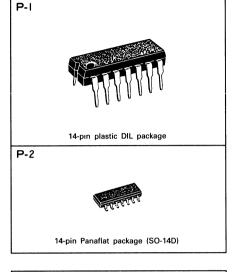
table

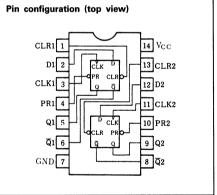
4. \overline{Q}_0 : Q level prior to determination of input condition shown in

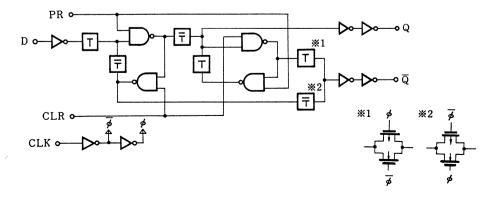
table

5. H*: When preset and clear are low, Q and Q are HIGH; however, when preset and clear simultaneously change to HIGH, requirements of Q and Q cannot be predicted.

■ Logic Diagram (1 Gate)







■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit	
Supply voltage			V_{CC}	-0.5~+7.0	V	
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V	
Input protect	ion diode current		I _{IK}	±20	mA	
Output paras	itic diode current		Iok	±20	mA	
Output curre	Output current			±25	mA	
Supply curre	Supply current			±50	mA	
Storage temp	oerature range		Tstg	-65 ∼+150	$^{\circ}$	
	MN74HC74	Ta=-40~+60℃	P_{D}	400	mW	
Power	MIN/4HC/4	Ta=+60~+85°C	FD	Decrease to 200mW at the rate of 8mW/°C	m vv	
dissipation	MN74HC74S	Ta=-40~+60°C	D-	275		
	MN/40C/45	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	v
Operating temperature range	TA		-40~+ 85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

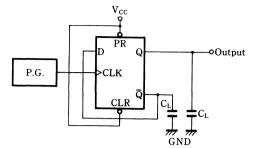
■ DC Characteristics (GND=0V)

		37	Tes	st Conditio	ons		T	emperatu	ire		
Parameter	Symbol	V _{cc} (V)	Vı	Io		,	Γa=25 °	C	Ta=-40)~+85℃	Unit
		(V)	V I	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		Unit V V
Input HIGH voltage	V_{IH}	4.5				3.15		İ	3.15		V
		6.0				4.2]	4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2	1.2		
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μΑ	4.4	4.5	1	4.4		
Output HIGH voltage	V_{OH}	6.0 or -20.0 μ A 5.9 6.0 5	5.9		V						
		4.5	VIL	-4.0	mA	3.86			3.76		V
		6.0		-5.2	mA	5.36	1		5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_{\rm I} = V_{\rm CO}$	c or GNI	$D, I_0=0$			4.0		40.0	μA

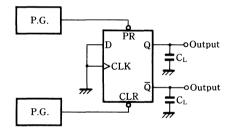
■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

						emperat			
Parameter	Symbol	Vcc	$V_{CC} \ (V)$ Test Conditions						
				Ta=25℃		Ta=-4)~+85℃	Unit
		,		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	tTHL	4.5			7	15		19	ns
		6.0			6	13		16	
Description times		2.0			32	150		190	
Propagation time	tplH	4.5			14	30		38	ns
$CLK \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0			11	26		33	
Dunna mation time		2.0			32	150		190	·
Propagation time	tPHL	4.5			14	30		38	ns
$CLK \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0			11	26		33	
D		2.0			32	150		190	
Propagation time	tplH	4.5			14	30		38	ns
$PR,CLR \rightarrow Q,\overline{Q} (L \rightarrow H)$		6.0			10	26		33	
D		2.0			32	150		190	
Propagation time	tPHL	4.5			13	30		38	ns
$PR,CLR \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0			10	26		33	
		2.0			7	75		95	
Minimum Set-up time	tsu	4.5		1	4	15	}	19	ns
		6.0			3	13		16	
		2.0			_	0		0	
Minimum Hold time	th	4.5			_	0		0	ns
	·	6.0			_	0		0	
		2.0			26	75		95	
Minimum pulse width	t _w	4.5			9	15		19	ns
PR, CLR		6.0			7	13		16	
		2.0	.,		5	75		95	
Minimum recovery time	trem	4.5			4	15		19	ns
PR, CLR	-10	6.0			2	13		16	
		2.0		6	20		4		
Maximum clock	f max.	4.5		30	58		24		MH z
frequency	¹ max.	6.0		35	70		28		1-111 C

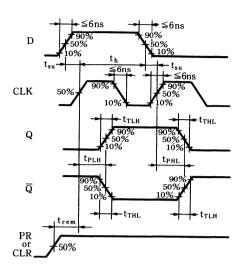
- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , t_{su} , t_{max} , t_{PLH}/t_{PHL} (CLK \rightarrow Q, \overline{Q}), t_{rem} , t_h 1. Measuring Circuit (t_{PLH} , t_{PHL})



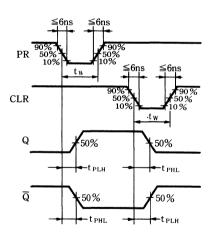
[2] t_{PLH}/t_{PHL} (CLR \rightarrow Q, \overline{Q}), t_{W} 1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



2. Waveforms



MN74HC75/MN74HC75S

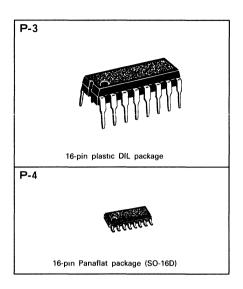
4-Bit Bistable Latch

■ Description

MN74HC75/MN74HC75S are 4-bit bistable latches with Q, \overline{Q} output. These are suited for temporary binary data memory circuits between the data processing unit and the I/O, or between display units. Data at data input (D) is transferred to output Q, when enable pin (G) is "H"; output Q follows the data input state so long as the enable is "H". When the enable becomes "L", output Q indicates the data input state when the enable changes from "H" to "L".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



■ Truth table

In	put	O	utput
D	G	Q	Q
L	Н	L	Н
Н	Н	Н	L
×	L	Q0	$\overline{\overline{Q}}0$

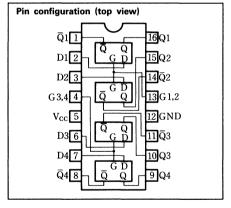
Note:

1. ×: Either HIGH or LOW; it doesn't matter

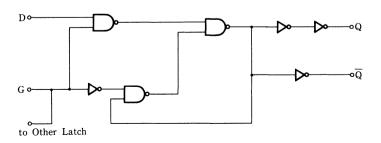
2. Q_0 : Q level prior to determination of input condition shown

in table

3. \overline{Q}_O : \overline{Q} level prior to determination of input condition shown in table



■ Logic Diagram



■ Absolute Maximum Ratings

	Parameter		Symbol	Rating	Unit												
Supply voltag	voltage		voltage		voltage		voltage		tage		voltage		ply voltage		$V_{\rm cc}$	-0.5~+7.0	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm cc} + 0.5$	V												
Input protect	tion diode current		I _{IK}	±20	mA												
Output paras	Output parasitic diode current			±20	mA												
Output curre	Output current			ut current		ıt current		Io	±25	mA							
Supply curre	current		I _{CC} , I _{GND}	±50	mA												
Storage temp	ge temperature range		Tstg	−65~+150	°C												
	MN74HC75	Ta=-40~+60℃	P_{D}	400	mW												
Power	MN/4HC/3	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 8mW/°C	m vv												
dissipation	MN74HC75S	Ta=-40~+60°C	D-	275													
	MN/40C/55	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW												

■ Operating Conditions

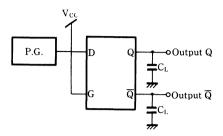
Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	v
Operating temperature range	TA		-40~+ 85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

		·	Те	st Conditi	ons		T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vı			•	Ta=25°C			0~+85℃	Unit
		(•)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
Input LOW voltage		2.0						0.3		0.3	
	VIL	4.5	1					0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	V _{OH}	4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	Icc	6.0	$V_I = V_C$	c or GN	$D, I_0=0$			4.0		40.0	μA

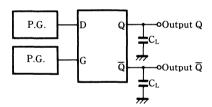
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

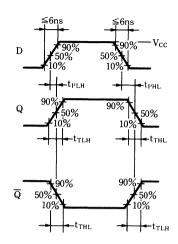
		Vcc		ļ		mperat	,		
Parameter	Symbol	(V)	Test Conditions		Ta=25℃		$T_a=-4$	0~+85℃	Unit
		()		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
-		6.0			7	13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0			5	13		16	
		2.0			İ	100		125	
Minimum Set-up time	t su	4.5			8	20		25	ns
		6.0				17		21	
		2.0			_	0		0	
Minimum Hold time	t _h	4.5			_	0		0	ns
		6.0				0		0	
		2.0				75		95	
Minimum recovery time	t _w	4.5			6	15		19	ns
**************************************		6.0				13		16	
Propagation time		2.0				125		155	
D→Q (L→H)	tPLH	4.5			14	25		31	ns
		6.0				21		26	
Propagation time		2.0				125		155	
D→Q (H→L)	tPHL	4.5			14	25		31	ns
D · Q (II · L)		6.0				21		26	
Propagation time		2.0				100		125	
$D \rightarrow \overline{Q} (L \rightarrow H)$	tplH	4.5			14	20		25	ns
D-4 (L-11)		6.0				17		21	
Propagation time		2.0				100		125	
$D \rightarrow \overline{Q} (H \rightarrow L)$	tPHL	4.5			14	20		25	ns
D · Q (II · L)		6.0				17		21	
Propagation time		2.0				125		155	
G→Q (L→H)	t _{PLH}	4.5			16	25		31	ns
G 4 (2 II)		6.0				21		26	
Propagation time		2.0				125		155	
G→Q (H→L)	tPHL	4.5			17	25		31	ns
G (H *L)		6.0				21		26	
Propagation time		2.0				125		155	
$G \rightarrow \overline{\mathbb{Q}} (L \rightarrow H)$	tplh	4.5			17	25		31	ns
G 'W (L→n)		6.0				21		26	
Propagation time		2.0				125		155	
$G \rightarrow \overline{Q} (H \rightarrow L)$	tPHL	4.5			14	25		31	ns
G ~W (n→L)		6.0				21		26	

- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , t_{su} , f_{max} , t_{PLH}/t_{PHL} (CLK \rightarrow Q, \overline{Q}), t_{rem} , t_h
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

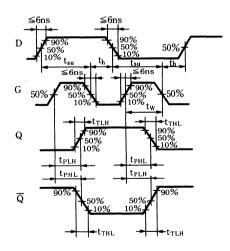


- [2] t_{PLH}/t_{PHL} (CLR \rightarrow Q, \overline{Q}), t_W
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})





2. Waveforms





MN74HC76/MN74HC76S

Dual J-K Flip-Flops with Preset and Clear

■ Description

MN74HC76/MN74HC76S contain two J-K flip-flop circuits with preset and clear. Each flip-flop has independent J, K, clear, preset, clock input and complementary Q and \overline{Q} outputs. Input data is transferred to the output on the negative going edge of the clock pulse. Preset and clear operate at low level regardless of the clock. Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to CMOS, and an operation speed of LS TTL. Each output can directly drive LS TTL 10-inputs. Resistor and diode are provided between the $\rm V_{CC}$ and GND to protect the input and output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Truth table

		Input			Ou	tput
PR	CLR	CLK	J	K	Q	\overline{Q}
L	Н	×	×	×	Н	L
Н	L	×	×	×	L	Н
L	L	×	×	×	H*	H*
Н	Н	X	L	L	Q0	$\overline{Q}0$
Н	Н	Ž	Н	L	Н	L
Н	Н	X	L	Н	L	Н
Н	Н	×	Н	Н	Toggle	
Н	Н	Н	×	×	Q0	Q0

Note:

1. ×: Either HIGH or LOW; it doesn't matter

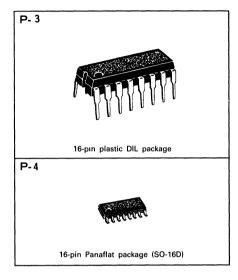
2. \(\cdot\): Rise of negative direction

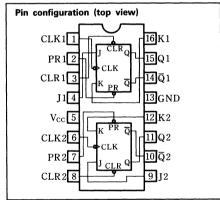
3. Q₀: Q level prior to determination of input condition shown in

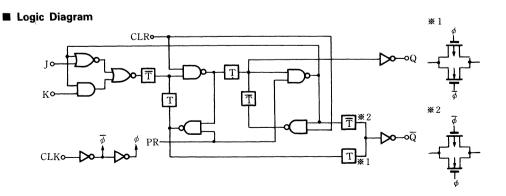
4. \overline{Q}_{O} : \overline{Q} level prior to determination of input condition shown in table

5. Toggle: With `_ change, output becomes a complement of the previous condition

 H*: When preset and clear are low, Q and Q are HIGH; however, when preset and clear simultaneously change to HIGH, requirements of Q and Q cannot be predicted.







■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit	
Supply voltage	де		V_{CC}	-0.5~+7.0	V	
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V	
Input protect	tion diode current		I _{IK}	±20	mA	
Output paras	sitic diode current		Iok	±20	mA	
Output curre	t current		Io	±25	mA	
Supply curre	current		Icc, I _{GND}	±50	mA	
Storage temp	perature range		Tstg	-65~+150	$^{\circ}$	
	MN74HC76	Ta=-40~+60℃	P_{D}	400	mW	
Power dissipation	MN/4HC/6	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 8mW/°C		
	MN74HC76S	Ta=-40~+60℃	D-	275	mW	
	WIN14fiC/05	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	III VV	

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	T _A		−40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

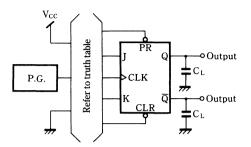
Dammadan		V_{CC}	Test Conditions			Te	emperatu	re			
Parameter	Symbol	(V)	Vı	_		,	Γa=25°		Ta=-40)~+85℃	Unit
		(v)	l VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0	ĺ			4.2			4.2		
The second second		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
	Vон	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	V _I =V _{CC} or GND				±0.1		±1.0	μA	
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	or GN	$D, I_0=0$			4.0		40.0	μA

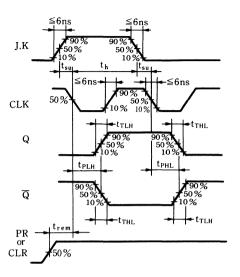


 \blacksquare AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

		37			7	empera	ture		
Parameter	Symbol	Vcc (V)	Test Conditions	•	Ta=25℃	;	Ta = -40	~+85℃	Unit
		(• /		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	t TLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t THL	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0				150		190	
Propagation time	t PLH	4.5			18	30		38	ns
$CLK \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0				26		33	
D		2.0	anna ann an Aireann ann an Aireann ann an Aireann an Aireann an Aireann an Aireann an Aireann an Aireann an Ai			150		190	
Propagation time	t PHL	4.5		1	17	30		38	ns
$CLK \rightarrow Q, \overline{Q}(H \rightarrow L)$		6.0				26		30	
		2.0				175		220	
Propagation time	t PLH	4.5			20	35		44	ns
$PR,CLR \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0				30		37	
-		2.0				175		220	
Propagation time	t PHL	4.5			19	35		44	ns
$PR,CLR \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0				30		37	
		2.0				75		95	
Propagation time	t w	4.5			8	15	İ	19	ns
PR,CLR		6.0				13		16	
		2.0				100	1	125	
Minimum Set-up time	tsu	4.5			9	20		25	ns
		6.0				17		21	
		2.0				0		0	
Minimum Hold time	th	4.5			_	0		0	ns
		6.0			_	0		0	
		2.0				75	 	95	
Minimum recovery time	trem	4.5			1	15		19	ns
•		6.0				13		16	
		2.0		6			4		
Maximum clock	f max.	4.5		30	50		24		MHz
equency	- max.	6.0		35			28		

- Switching Time Measuring Circuit and Waveforms
- [1] $t_{TLH}\text{, }t_{THL}\text{, }t_{su}\text{, }f_{max}\text{, }t_{PLH}/t_{PHL}$ (CLK \rightarrow Q, $\overline{\text{Q}}\text{), }t_{rem}\text{, }t_{h}$
 - 1. Measuring Circuit (tpl.H, tpHL)

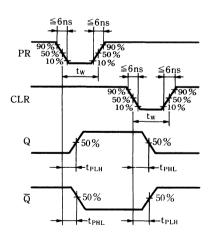




- [2] t_{PLH}/t_{PHL} (CLR \rightarrow Q, \overline{Q}), t_W
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

P.G. P.G. P.G. P.G. Output CLK CLR CLR CLR Output

2. Waveforms





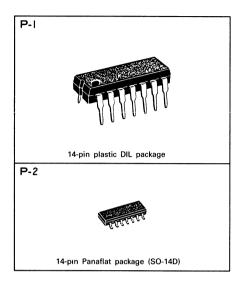
MN74HC77/MN74HC77S

4-Bit Bistable Latch

■ Description

MN74HC77/MN74HC77S are 4-bit bistable latches. These are suited for temporary binary data memory circuits between the data processing unit and the I/O, or between display units. Data at data input (D) are transferred to output Q, when enable pin (G) is "H"; output Q follows the data input state so long as the enable is "H". When the enable becomes "L", output is maintained as is until when the enable becomes "H". Output Q indicates the data input state when the enable changes from "H" to "L".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



■ Truth table

In	put	Output
D	G	Q
L	Н	L
Н	Н	Н
×	L	Q0

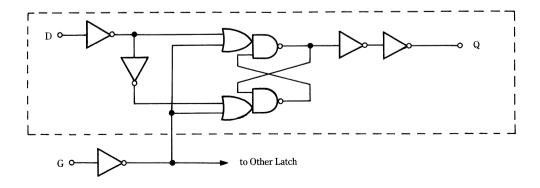
Note:

1. x: Either HIGH or LOW; it doesn't matter

2. Q_O: Q level prior to determination of input condition shown in

table

■ Logic Diagram (1 gate)



■ Absolute Maximum Ratings

	Parameter	r	Symbol	Rating	Unit		
Supply voltag	ge		$V_{\rm cc}$	$-0.5\sim+7.0$	V		
Input/output	t/output voltage		V _I , V _o	$-0.5 \sim V_{\rm CC} + 0.5$	V		
Input protect	ion diode current		I _{IK}	±20	mA		
Output paras	itic diode current		Іок	±20	mA		
Output curre	rent		t current		Io	±25	mA
Supply curre	current		I _{CC} , I _{GND}	±50	mA		
Storage temp	erature range		Tstg	−65~+150	c		
	MN74HC77	Ta=-40~+60℃	PD	400	mW		
Power	MN/4HC//	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 8mW/°C	111 VV		
dissipation	MN74HC77S	Ta=-40~+60°C	D-	275	mW		
	MN/4nC//S	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	III VV		

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	v
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	T_{A}		-40~+85	C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

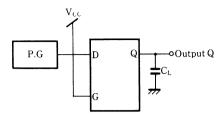
		3.7	Te	st Condition	ons		T	emperatu	re		
Parameter	Symbol	Vcc	Vı	Io		,	Γa=25°	2	Ta=-40)~+85℃	Unit
		(V)	V 1	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15		1	3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V_{IH}	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	VoH	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μ A		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Ιι	6.0	$V_{\rm I} = V_{\rm C}$	c or GN	D			±0.1		±1.0	μΑ
Quiescent supply current	I_{CC}	6.0	$V_I = V_{C}$	c or GNI	$I_0=0$			4.0		40.0	μA

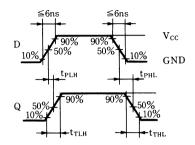


■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

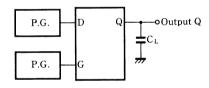
		V_{CC}			T	emperat	ure		
Parameter	Symbol	(V)	Test Conditions		Γa=25°C	;	Ta=-4	0~+85℃	Unit
		(, ,		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	tTHL	4.5			7	15	l	19	ns
		6.0			6	13		16	
		2.0				100		125	
Minimum Set-up time	tsu	4.5			2	20		25	ns
		6.0				17		21	
		2.0			_	0		0	
Minimum Hold time	th	4.5			_	0		0	ns
		6.0			_	0		0	
		2.0				75		95	
Minimum pulse width	t w	4.5			6	15		19	ns
		6.0		ļ		13		16	
Propagation time	1	2.0				125		155	
$D \rightarrow Q (L \rightarrow H)$	tPLH	4.5			15	25		31	ns
D→Q (L→H)		6.0				21		26	
D		2.0				125		155	
Propagation time	tPHL	4.5			14	25		31	ns
$D \rightarrow Q (H \rightarrow L)$		6.0				21		26	
D		2.0				125		155	
Propagation time	tplH	4.5			11	25		31	ns
$G \rightarrow Q(L \rightarrow H)$		6.0				21		26	
D		2.0		1		125		155	
Propagation time	tPHL	4.5			13	25		31	ns
$G \rightarrow Q (H \rightarrow L)$		6.0				21		26	

- Switching Time Measuring Circuit and Waveforms
- $[1] \ t_{TLH} \text{,} \ t_{THL} \text{,} \ t_{su} \text{,} \ f_{max} \text{,} \ t_{PLH} / t_{PHL} \ (CLK \rightarrow Q, \ \overline{Q}) \text{,} \ t_{rem} \text{,} \ t_h$
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

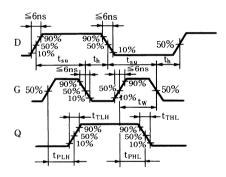




- [2] t_{PLH}/t_{PHL} (CLR \rightarrow Q, \overline{Q}), t_W
 - 1. Measuring Circuit (t_{PLH},t_{PHL})



2. Waveforms



MN74HC86/MN74HC86S

Quad 2-Input Exclusive OR Gate

■ Description

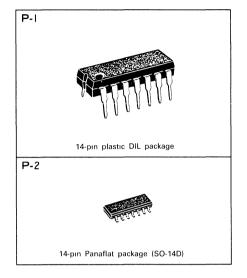
MN74HC86/MN74HC86S contain quad 2-input exclusive OR (XOR) gate.

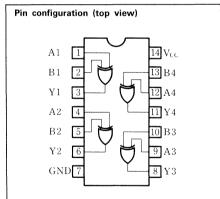
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL; LS TTL 10-inputs can be directly driven.

A resistor and diode are provided in $V_{\rm CC}$ and GND to protect the input/output from damge by static electricity. Same pin configuration and function as the standard 54LS/74LS.

■ Logic Diagram (1 gate)







■ Absolute Maximum Ratings

	Paramete	er	Symbol	Rating	Unit
Supply volta	Supply voltage			$-0.5 \sim +7.0$	V
Input/output voltage			$V_{\rm I}, V_{\rm O}$	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	Input protection diode current			±20	mA
Output para	sitic diode current		Iok	±20	mA
Output curre	Output current			±25	mA
Supply curre	ent		I_{CC}, I_{GND}	±50	mA
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$
	MN74HC86	Ta=-40~+60°C	P_{D}	400	mW
Power $Ta=+60\sim+85^{\circ}$		I PD	Decrease to 200mW at the rate of 8mW/°C	mvv	
dissipation	dissipation MN74HC86S $Ta=-40\sim+60^{\circ}$		D.	275	VA/
$T_a = +60 \sim +85^{\circ}$		P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	v
Input/output voltage	$V_{\rm I}, V_{\rm O}$		$0 \sim V_{\rm CC}$	v
Operating temperature range	TA		-40 ∼+85	°C
		2.0	0~1000	ns
Input rise and fall time	t_r, t_f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		V _{cc}	Те	st Conditi	ons		Т	emperat	ure		
Parameter	Symbol		Vı	,		,	Ta=25°	C	Ta=-4()~+85℃	Unit
		(V)	V I	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		v
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1	į	0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	$I_{\rm I}$	6.0	$V_{\rm I} = V_{\rm C}$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	or GNI	$D,I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

					Temperature					
Parameter	Symbol	V _{CC}	Test Conditions		Ta=25℃)~+85℃	Unit	
		(V)		min.	typ.	max.	min.	max.		
		2.0			25	75		95		
Output rise time	tTLH	4.5			8	15		19	ns	
		6.0			7	13		16		
		2.0			20	75		95		
Output fall time	t _{THL}	4.5			7	15		19	ns	
		6.0			6	13		16		
		2.0			25	75		95		
Propagation time	t _{PLH}	4.5			8	15		19	ns	
$(L \rightarrow H)$		6.0			7	13]	16		
		2.0			25	75		95		
Propagation time	t _{PHL}	4.5			8	15		19	ns	
$(H \rightarrow L)$		6.0			7	13		16		



MN74HC107/MN74HC107S

Dual J-K Flip-Flops with Clear

■ Description

MN74HC107/MN74HC107S contain dual J-K flip-flop with clear, and each flip-flop has independent J, K, clock, clear input and complementary output Q and \overline{Q} . Input data is transferred to the output on the negative-going edge of the clock pulse. Clear operates on the low level regardless of the clock.

Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL; LS TTL 10-inputs can be directly driven.

A resistor and diode are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS.

P-I 14-pin plastic DIL package P-2 14-pin Panaflat package (SO-14D)

■ Truth table

	In	Output			
CLR	CLK	J	K	Q	$\overline{\overline{Q}}$
L	×	×	×	L	Н
Н	عر	L	L	Qo	$\overline{\overline{Q}}_{o}$
Н	74_	Н	L	Н	L
Н	7	L	Н	L	Н
Н	7_	Н	Н	Tog	gle
Н	Н	×	×	Qo	$\overline{\overline{Q}}_{o}$

Note:

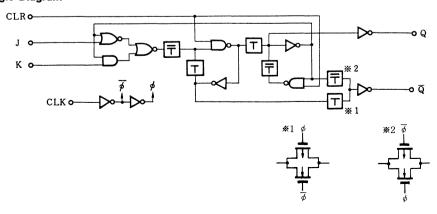
1. \(\tag{\chi}\): Data input is transferred to output on the negative-going edge from HIGH to LOW of the clock

2. ×: Either HIGH or LOW; it doesn't matter

3. Q_O : (\overline{Q}_O) : $Q(\overline{Q})$ level prior to determination of input condition shown in table

4. Toggle: With 🥄 change, output becomes a complement of the previous condition

■ Logic Diagram



■ Absolute Maximum Ratings

	Parameter	•	Symbol	Rating	Unit					
Supply voltag	Supply voltage			ltage		pply voltage		V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V					
Input protect	Input protection diode current			tection diode current		I _{IK}	±20	mA		
Output paras	itic diode current		Іок	±20	mA					
Output curre	Output current			±25	mA					
Supply curren	nt		Icc, Ignd	±50	mA					
Storage temp	perature range		Tstg	-65~+150	°C					
	MN74HC107	Ta=-40~+60℃	D.	400	mW					
Power	Power $Ta=+60\sim+85^{\circ}$		P_D	Decrease to 200mW at the rate of 8mW/°C	III VV					
dissipation	dissipation $Ta = -40 \sim +60 \text{C}$		D	275	W					
$T_a = +60 \sim +85 \text{°C}$		P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	mW						

■ Operating Conditions

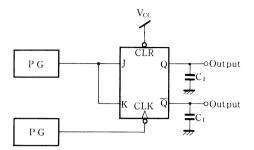
Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

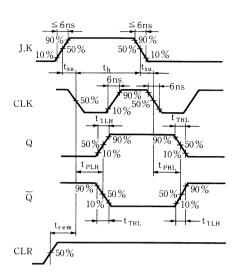
		V_{CC}	Те	st Condition	ons		Te	emperatu	re		
Parameter	Symbol	(V)	17			•	Γa=25°		Ta=-40	0~+85℃	Unit
		(•)	VI	I_0	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OL}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36		1	5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μΑ		0.0	0.1		0.1	V
,,g.		4.5	V _{II} .	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_1	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GNI	$0, I_0=0$			4.0		40.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

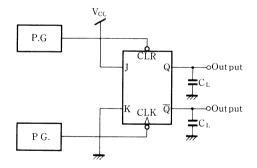
		17			Te	emperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions	7	Γa = 25°C	;	$T_a = -4$	0~+85°C	Unit
		(*/		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
D		2.0			34	125		155	
Propagation time	t _{PLH}	4.5			14	25		31	ns
$CLK \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0			11	21		26	
Propagation time		2.0			37	125		155	
CLK \rightarrow Q, \overline{Q} (H \rightarrow L)	t PHL	4.5			13	25		31	ns
$CLK\rightarrow Q, Q (H\rightarrow L)$		6.0			10	21		26	
Propagation time		2.0			48	150		190	
Propagation time $CLR \rightarrow \overline{Q} (L \rightarrow H)$	t PLH	4.5			19	30		38	ns
CLR→Q (L→H)		6.0			15	26		33	
Propagation time		2.0			42	125		155	
	t PHL	4.5			15	25		31	ns
$CLR \rightarrow Q (H \rightarrow L)$		6.0			13	21		26	
		2.0			16	75		95	
Minimum Set-up time	tsu	4.5			6	15		19	ns
		6.0			5	13		16	
		2.0			_	0		0	
Minimum Hold time	t h	4.5			-	0		0	ns
		6.0			-	0		0	
Minimum pulse width		2.0			17	75		95	
CLR	t w	4.5			8	15		19	ns
CLI		6.0			6	13		16	
		2.0			15	75		95	
Minimum recovery time	trem	4.5			4	15		19	ns
		6.0			2	13		16	
Mi		2.0		6	24		4		
Maximum clock	f max.	4.5		30	64		24		MH z
frequency		6.0		35	83		28		

- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , t_{su} , f_{max} , t_{PLH}/t_{PHL} (CLK \rightarrow Q, \overline{Q}), t_{rem} , t_h
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})

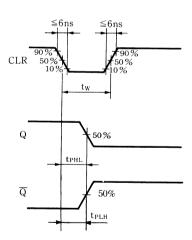




- [2] t_{PLH}/t_{PHL} (CLR \rightarrow Q, \overline{Q}), t_W
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HC109/MN74HC109S

Dual J-K Flip-Flops with Preset and Clear

■ Description

MN74HC109/MN74HC109S contain dual J- \overline{K} flip-flop with preset and clear and each flip-flop has independent J, \overline{K} , clock, clear, preset input and complementary output Q and \overline{Q} . Input data is transferred to the output on the rising edge of the clock pulse. Clear and preset operatate on the low level regardless of the clock. Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL; LS TTL 10-inputs can be directly driven.

A Resistors and diode are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Truth Table

		Input			Outpu	t
PR	CLR	CLK	J	K	Q	$\overline{\mathbf{Q}}$
L	Н	×	×	×	Н	L
Н	L	×	×	×	L	Н
L	L	×	×	×	H*	H *
Н	Н	₹	L	L	L	Н
Н	Н	ℱ	Н	L	Tog	gle
Н	Н	₹	L	Н	Q_{o}	$\overline{\mathrm{Q}}_{\mathrm{o}}$
Н	Н	5	Н	Н	Н	L
Н	Н	L	×	×	Q_{o}	\overline{Q}_{0}

Note:

1. ×: Either HIGH or LOW; it doesn't matter

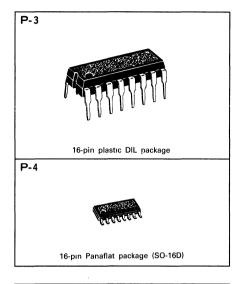
2. 1: Rise of positive direction

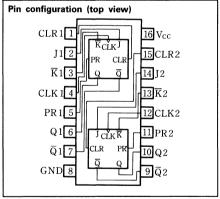
3. Q_O: Q level prior to determination of input condition shown in

4. \overline{Q}_{O} : Q level prior to determination of input condition shown in table

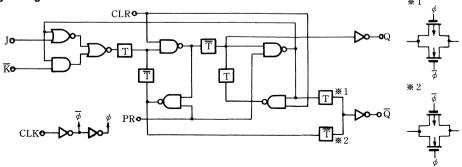
5. Toggle: With $\mathcal S$ change, output becomes a complement of the previous condition

5. H*: When preset and clear are low, Q and Q are HIGH; however, when preset and clear simultaneously change to HIGH, requirements of Q and Q cannot be predicted.









■ Absolute Maximum Ratings

	Parameter		Symbol	Rating	Unit									
Supply voltage	Supply voltage			tage		age		voltage		tage		$V_{\rm CC}$	$-0.5 \sim +7.0$	V
Input/output voltage			V _I , V _O	0.5~V _{CC} +0.5	V									
Input protection diode current			I _{IK}	± 20	mA									
Output parasitic diode current			Ioĸ	±20	mA									
Output curre	Output current			current		Io	±25	mA						
Supply curre	rrent		I _{CC} , I _{GND}	±50	mA									
Storage temp	perature range		Tstg	-65~+150	°C									
	MN74HC109	Ta=-40~+60°C	P_{D}	400	mW									
Power	MN74HC109	Ta=+60~+85 ℃	Fρ	Decrease to 200mW at the rate of 8mW/°C	III VV									
dissipation	MN74HC109S	Ta=-40~+60°C	P_{D}	275	mW									
	MIN/4/IC1095	Ta=+60~+85°C	I I	Decrease to 200mW at the rate of 3.8mW/°C	111 44									

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm CC}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0∼V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
Input rise and fall time		2.0	0~1000	ns
	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

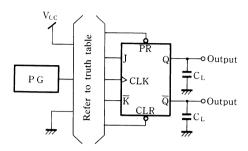
		.,	Te	st Conditi	ons		Te	emperatu	re		
Parameter	Symbol	Vcc	W	Io	τ.		Γa=25°	2	Ta=-40)~+85℃	Unit
		(V)	V _I	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5		,		3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
	V _{он}	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_I = V_C$	c or GNI	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	or GNI	O, I ₀ =0			4.0		40.0	μΑ



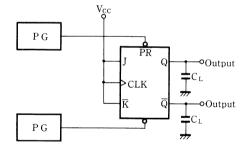
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

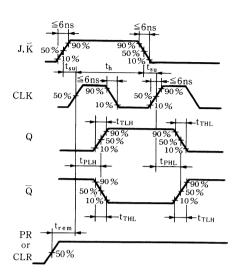
		$V_{\rm CC}$			Te	mperatu	ire		
Parameter	Symbol	1 1	Test Conditions	Т	`a=25℃		$T_a = -40$	~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5				15	1	19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	tTHL	4.5				15		19	ns
		6.0				13		16	
D		2.0				125		155	
Propagation time	t_{PLH}	4.5				25		31	ns
$CLK \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0				21		26	
Б		2.0				125		155	
Propagation time	tpHL	4.5			[25		31	ns
$CLK \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0			1	21	}	26	
D		2.0				125		155	
Propagation time	tPLH	4.5				25		31	ns
PR, CLR \rightarrow Q, \overline{Q} (L \rightarrow H)		6.0				21		26	
D		2.0				125		155	
Propagation time	tPHL	4.5				25		31	ns
$PR, CLR \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0				21		26	
		2.0				75		95	
Minimum pulse width	t _w	4.5				15		19	ns
PR,CLR		6.0				13		16	
4.400		2.0				100		125	
Minimum Set-up time	tsu	4.5				20		25	ns
		6.0				17		21	
The state of the s		2.0			_	0		0	
Minimum Hold time	t _h	4.5			_	0		0	ns
		6.0			_	0		0	
Mınimum recovery tıme		2.0				75		95	
	trem	4.5				15		19	ns
		6.0				13		16	
		2.0	The second secon	6			4		
Maximum clock frequency	fmax	4.5		30			24		MH_{Z}
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , t_{su} , f_{max} , t_{PLH}/t_{PHL} (CLK \rightarrow Q, \overline{Q}), t_{rem} , t_h
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

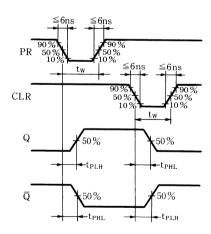


- [2] t_{PLH}/t_{PHL} (CLR \rightarrow Q, \overline{Q}), t_W
 - 1. Measuring Circuit (t_{PLH},t_{PHL})





2. Waveforms





MN74HC112/MN74HC112S

Dual J-K Flip-Flops with Preset and Clear

■ Description

MN74HC112/MN74HC112S contain dual J-K flip-flop with clear, and each flip-flop has independent J, K, preset, clock, clear input and complementary output Q and \overline{Q} . Input data is transferred to the output on the negative going edge of the clock pulse. Clear operates on the low level regardless of the clock. Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL; LS TTL 10-inputs can be directly driven.

A Resistors and diode are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3 16-pin plastic DIL package P-4 16-pin Panaflat package (SO-16D)

■ Truth Table

	Iı	nput			Outp	ut
PR	CLR	CLK	J	K	Q	\overline{Q}
L	Н	×	×	×	Н	L
Н	L	×	×	×	L	Н
L	L	×	×	×	H *	H *
Н	Н	74	L	L	Q_{o}	\overline{Q}_{0}
Н	Н	Z	Н	L	Н	L
Н	Н	٦٧	L	Н	L	Н
Н	Н	72	Н	Н	Toggle	
Н	Н	Н	×	×	Qo	\overline{Q}_0

Note:

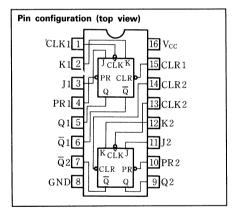
1. ×: Either HIGH or LOW; it doesn't matter

2. \tau: Rise of negative direction

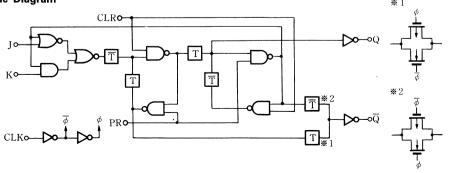
3. Q₀: Qlevel prior to determination of input condition shown in table
 4. Q₀: Qlevel prior to determination of input condition shown in table

5. Toggle: With > change, output becomes a complement of the previous condition

5. H*: When preset and clear are low, Q and Q are HIGH; however, when preset and clear simultaneously change to HIGH, requirements of Q and Q cannot be predicted.



■ Logic Diagram



■ Absolute Maximum Ratings

	Parameter	•	Symbol	Rating	Unit			
Supply voltag	Supply voltage			−0.5 ~+7.0	V			
Input/output voltage			V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V			
Input protection diode current			I _{IK}	±20	mA			
Output parasitic diode current			Ioĸ	±20	mA			
Output current			Io	±25	mA			
Supply curre	Supply current			rrent		I _{CC} , I _{GND}	±50	mA
Storage temp	perature range		Tstg	-65~+150	$^{\circ}$			
	MN74HC112	Ta=-40~+60℃	P_{D}	400	mW			
Power		Ta=+60~+85℃	Iυ	Decrease to 200mW at the rate of 8mW/°C	111 VV			
dissipation	MN74HC112S	Ta=-40~+60℃	P_D	275	тW			
	MN/4HC1125	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 3.8mW/°C	III VV			

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm CC}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~Vcc	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

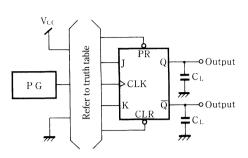
		.,	Te	st Conditi	ons		Te	emperatu	re		
Parameter	Symbol	Vcc	Vı	T		,	Γa=25 °	C	Ta=-40	0~+85℃	Unit
		(V)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
	V _{OH}	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26)	
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{C}$	c or GNI	$I_0=0$			4.0		40.0	μA

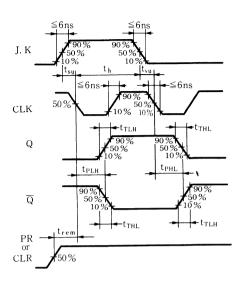


■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

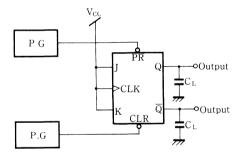
		N/			Te	mperati	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions	7	Γa = 25°C	,	$T_a = -40$)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
D		2.0				125		155	
Propagation time	tPLH	4.5			16	25		31	ns
$CLK \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0				21		26	
		2.0				125		155	
Propagation time	tpHL	4.5			16	25		31	ns
$CLK \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0				21		26	
	*****	2.0				125		155	
Propagation time	tPLH	4.5			17	25		31	ns
$PR,CLR \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0				21		26	
-		2.0				125		155	
Propagation time	tPHL	4.5			19	25		31	ns
$PR,CLR \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0				21		26	
		2.0				75		95	
Mınımum pulse width	t w	4.5			7	15		19	ns
PR,CLR		6.0				13		16	
		2.0				100		125	
Minimum Set-up time	t su	4.5			7	20		25	ns
		6.0				17		21	
		2.0				0		0	
Minimum Hold time	th	4.5			_	0		0	ns
	-	6.0			_	0		0	
		2.0	, , , , , , , , , , , , , , , , , , ,			75		95	
Mınımum recovery time	trem	4.5			1	15		19	ns
		6.0				13		16	
		2.0		6			4		
Maxımum clock frequency	f _{max} .	4.5		30	59		24		MH_{Z}
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , t_{su} , f_{max} , t_{PLH}/t_{PHL} (CLK \rightarrow Q, \overline{Q}), t_{rem} , t_h
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

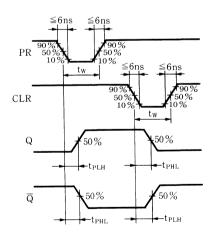




- [2] t_{PLH}/t_{PHL} (CLR \rightarrow Q, \overline{Q}), t_W
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms





MN74HC125/MN74HC125\$

Quad TRI-STATE Buffers

■ Description

MN74HC125/MN74HC125S are high-speed non-inverted buffers consisting of quad tri-state outputs. High-speed operation is possible for driving a large capacitance bus line owing to large current output. The gate can be controlled by tri-state input (C), when output becomes enabled at LOW. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $\rm V_{CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Truth Table

In	put	Output
С	A	Y
Н	×	Hı-Z
L	L	L
L	Н	Н

Note:

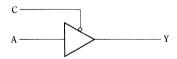
1. H: HIGH level

2. L: LOW level

3. ×: Either HIGH or LOW; doesn't matter.

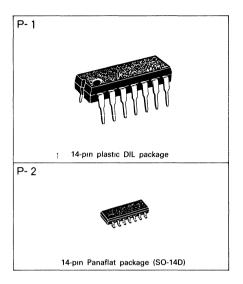
4. Hi-Z: Hi-Impeadance

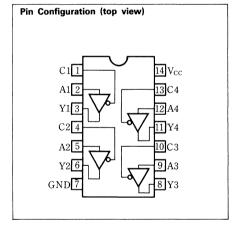
■ Logic Diagram



■ Absolute Maximum Ratings

	Paramet	er	Symbol	Rating	Unit	
Supply voltage	ply voltage		V _{CC}	-0.5~+7.0	V	
Input/output voltage			V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V	
Input protection diode current			I_{IK}	±20	mA	
Output parasitic diode current			I_{OK}	±20	mA	
Output current			$I_{\rm O}$	±35	mA	
Supply curre	rrent		I _{CC} , I _{GND}	±70	mA	
Storage temp	erature range		Tstg	−65~+150	°C	
	MN74HC125	Ta=-40~+60°C	D	400	mW	
Power	WIN74HC125	Ta=+60~+85°C	$ P_{\rm D}$	Decrease to 200mW at the rate of 8mW/°C		
dissipation MN74HC125S	Ta=-40~+60°C	ъ	275			
	WIN /4/1C1255	Ta=+60~+85°C	$P_{\rm D}$	Decrease to 200mW at the rate of 3.8mW/°C	mW	





■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating temperature range	V _{CC}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		V _{CC} =2.0V	0~1000	ns
Input rise and fall time	t _r , t _f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0V	0~400	ns

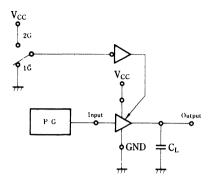
			Tes	t Conditio	ons		T	emperatu	re		ı
Parameter	Symbol	V _{CC} (V)	37	,			Ta=25°C		Ta=-40	~+85°C	Unit
		(*)	V _I	$I_{\rm O}$	Unit	min.	typ.	max.	min.	max.	
	·	2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	V
		2.0		-20.0	μΑ	1.9	2.0		1.9		V
	V _{OH}	4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		V
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	-6.0	mA	3.86			3.76		V
		6.0		-7.8	mA	5.36			5.26		V
		2.0		20.0	μΑ		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	V
		6.0		7.8	mA			0.32		0.37	V
Input current	I _I	6.0	V _I =	V _{CC} or G	ND			±0.1		±1.0	μΑ
3-state output off state current	I _{OZ}	6.0		=V _{IH} or V V _{CC} or G				±0.5		±5.0	μΑ
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CC}$	or GND	$I_0=0$			8.0		80.0	μ A



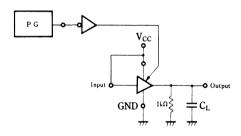
■ AC Characteristics (GND=0V, Input transistion tiem \leq 6ns, C_L=50pF)

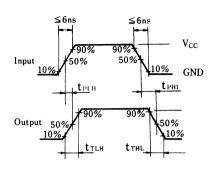
					T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta=-40	~+85°C	Unit
		(,,		min.	typ.	max.	min.	max.	
		2.0			19	75		95	
Output rise time	t _{TLH}	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			15	75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0			5	13		16	
~		2.0			15	75		95	
Propagation time (L→H)	t _{PLH}	4.5			9	15	1	19	ns
(2 11)		6.0			8	13		16	
		2.0			15	75		95	
Propagation time (H→L)	t _{PHL}	4.5			8	15		. 19	ns
(11 /2)		6.0			6	13		16	
		2.0			20	125		155	
Propagation time	t _{PHZ}	4.5	$R_L = 1k\Omega$		15	25		31	ns
(H→Z)		6.0			14	21		26	
		2.0			18	100		125	
Propagation time	t _{PLZ}	4.5	$R_L=1k\Omega$		12	20		25	ns
$(L \rightarrow Z)$		6.0			11	17		21	
		2.0			18	100		125	
Propagation time	t _{PZH}	4.5	$R_L = 1k\Omega$		10	20		25	ns
(Z→H)		6.0			8	17		21	
		2.0			28	100		125	
Propagation time	t_{PZL}	4.5	$R_L = 1k\Omega$		8	20		25	ns
(Z→L)	<u> </u>	6.0			7	17		21	

- Switching Time Measuring Circuit and Waveforms
- (1) ttlh, tthl, tplh, tphl
 - 1. Measuring Circuit

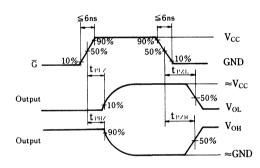


- $\{2\}$ t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit

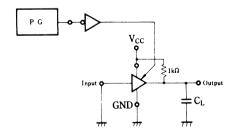




2. Waveforms (tphz, tpzh, tplz, tpzl)



- (3) tPLZ, tPZL
 - 1. Measuring Circuit





MN74HC126/MN74HC126S

Quad TRI-STATE Buffers

MN74HC126/MN74HC126S are high-speed non-inverted buffers consisting of quad tri-state outputs. High-speed operation is possible for driving a large capacitance bus line owing to large current output. The gate can be controlled by tri-state input (C), when output becomes enabled at HIGH. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Truth Table

Inp	ut	Output
С	A	Y
L	×	Hi-Z
Н	L	L
Н	Н	Н

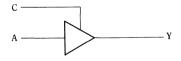
Note:

1. H: HIGH level 2. L: LOW level

3. ×: Either HIGH or LOW; doesn't matter.

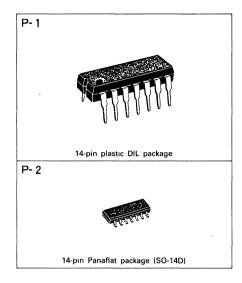
4. Hı-Z: Hı-Impeadance

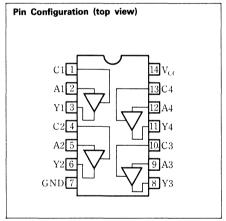
■ Logic Diagram



■ Absolute Maximum Ratings

	Paramete	er	Symbol	Rating	Unit
Supply voltage			V _{cc}	-0.5~+7.0	V
Input/output voltage			V _I , V _O	-0.5~V _{CC} +0.5	V
Input protection diode current			I _{IK}	±20	mA
Output parasitic diode current			I _{OK}	±20	mA
Output current			$I_{\rm O}$	±35	mA
Supply curren	nt		I _{CC} , I _{GND}	±70	mA
Storage temp	erature range		Tstg	−65~+150	°C
	MN74HC126 Ta=-40~+60°C		P _D	400	mW
Power	Power $Ta=+60\sim+85^{\circ}C$		T _D	Decrease to 200mW at the rate of 8mW/°C	111 VV
dissipation	dissipation $Ta = -40 \sim +60^{\circ}C$		D	275	mW
	WIN74HC1205	Ta=+60~+85°C	P _D	Decrease to 200mW at the rate of 3.8mW/°C	IIIVV





■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating uspply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	T _A		−40~+85	°C
		$V_{CC}=2.0V$	0~1000	ns
Input rise and fall time	t _r , t _f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0V	0~400	ns

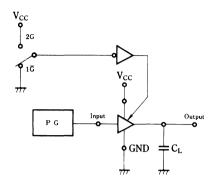
			Tes	t Condition	ons	Temperature					
Parameter	Symbol	V _{CC} (V)	37	,			Ta=25°C		Ta=-40	~+85°C	Unit
		(1)	V _I	$I_{\rm O}$	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	V
		2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		V
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-6.0	mA	3.86			3.76		V
		6.0		-7.8	mA	5.36			5.26		V
		2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V _{IH}	20.0	μΑ		0.0	0.1		0.1	V
Output LOW voltage	V_{OL}	6.0	or	20.0	μΑ		0.0	0.1		0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	V
		6.0		7.8	mA			0.32		0.37	V
Input current	I_{I}	6.0	V _I =	V _{CC} or G	ND			±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0		V _{IH} or V V _{CC} or G				±0.5		±5.0	μΑ
Quiescent supply current	Icc	6.0	$V_I = V_{CC}$	or GND	$I_{O}=0$			8.0		80.0	μA



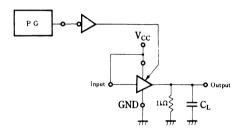
■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C_L=50pF)

	T	Ι			T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta=-40	~+85°C	Unit
		(.,		min.	typ.	max.	min.	max.	
		2.0			18	75		95	
Output irse time	t _{TLH}	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			13	75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0			5	13		16	
D		2.0			19	75		95	
Propagation time (L→H)	t _{PLH}	4.5			9	15		19	ns
		6.0			8	13		16	
		2.0			19	75		95	
Propagation time (H→L)	t _{PHL}	4.5			8	15		19	ns
(22 - 22)		6.0			6	13		16	
		2.0			20	125		155	
Propagation time	t _{PHZ}	4.5	$R_L=1k\Omega$		15	25		31	ns
(H→Z)		6.0			14	21		26	
		2.0			18	100		125	
Propagation time	t _{PLZ}	4.5	$R_L=1k\Omega$		12	20		25	ns
(L→Z)		6.0			11	17		21	
		2.0			19	100		125	
Propagation time	t _{PZH}	4.5	$R_L=1k\Omega$		10	20		25	ns
(Z→H)		6.0			8	17		21	
		2.0			20	100		125	
Propagation time	t _{PZL}	4.5	$R_L=1k\Omega$		8	20		25	ns
(Z→L)		6.0			7	17		21	

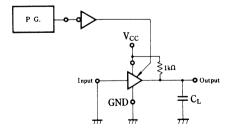
- Switching Time Measuring Circuit and Waveforms
- (1) ttlh, tthl, tplh, tphl
 - 1. Measuring Circuit

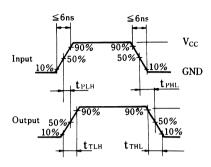


- (2) t_{PHZ}, t_{PZH}
 - 1. Measuring Circuit

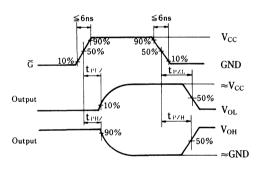


- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit





2. Waveforms (tphz, tpzh, tplz, tpzl)





MN74HC132/MN74HC132S

Quad 2-Input NAND Schmitt Triggers

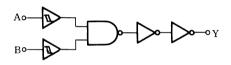
■ Description

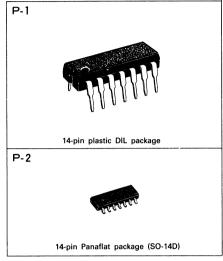
MN74HC132/MN74HC132S contain quad 2-input NAND with Schmitt triggers at all input terminals.

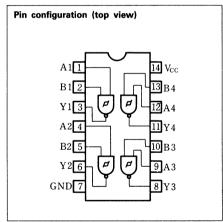
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Because the circuit threshold voltage differs $(V_{IH},\ V_{IL})$ when the input waveform rises and falls, wider applications are possible for the line reciever, waveform shaping and multi-vibrator in addition to the normal inverter.

Resistors and diode are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

■ Logic Diagram







■ Absolute Maximum Ratings

	Parameter	ſ	Symbol	Rating	Unit							
Supply voltage	Supply voltage			age		oltage		age		Vcc	$-0.5\sim+7.0$	V
Input/output	Input/output voltage			put voltage		t voltage		put voltage		V_1 , V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	Input protection diode current			± 20	mA							
Output paras	Output parasitic diode current			± 20	mA							
Output curre	Output current			± 25	mA							
Supply curre	ent	nt		± 50	mA							
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$							
	MN74HC132 Ta=−40~+60°C		Po	400	m W							
Power	Power $Ta = +60 \sim +85^{\circ}$ C		F))	Decrease to 200mW at the rate of 8mW/°C	m W							
dissipation	dissipation MN74HC132S $T_a = -40 \sim +60 \%$		D.	275	11'							
	MIN/4HC1325	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m W							

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V(c,	V
Operating temperature range	TA		-40~+85	°C

■ DC Characteristics (GND=0V)

		17	Te	st Conditi	ons		Te	mperatu	re		
Parameter	Symbol	(V)	Vı	Io		•	Γa=25 °C)	Ta=-40	~+85℃	Unit
		\ • / 	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V1 10	Unit	mın.	typ.	max.	mın.	max.	
		2.0		-20.0	μA	1.9	2.0		1.9	0.1	
		4.5	ViH	-20.0	μA	4.4	4.5		4.4	0.1	
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μΑ	5.9	6.0		5.9	0.1	V
		4.5	VII	-4.0	mA	3.86			3.76	0.37	
		6.0		-5.2	mA	5.36			5.26	0.37	
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	Vih	20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	Voi	6.0	or	20.0	μΑ		0.0	0.1		0.1	V
		4.5	V_{11}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_1	6.0	$V_{i} = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	Icc	6.0	$V_1 = V_0$.c or GNI), I ₀ =0			2.0		20.0	μA
		2.0				0.7	1.35	1.5	0.7	1.5	
	V_{T}^{+}	4.5				1.55	2.69	3.15	1.55	3.15	V
Input threshold voltage		6.0				2.1	3.55	4.2	2.1	4.2	
p		2.0				0.3	0.75	1.0	0.3	1.0	
	V_T -	4.5				0.9	1.85	2.45	0.9	2.45	V
		6.0				1.2	2.45	3.2	1.2	3.2	
		2.0				0.2	0.60	1.2	0.2	1.2	
Hysteresis voltage	V_{H}	4.5				0.4	0.84	2.1	0.4	2.1	V
		6.0				0.5	1.10	2.5	0.5	2.5	

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

		Vcc							
Parameter	Symbol	(V)	Test Conditions		Ta=25 °	2	Ta=-40)~+85℃	Unit
		• • • •		mın.	typ.	max.	mın.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	tTHL	4.5			6	15		19	ns
		6.0				13		16	
		2.0				100		125	
Propagation time $(L \rightarrow H)$	tplH	4.5			12	20		25	ns
(L → II)		6.0				17		21	
		2.0				100		125	
Propagation time $(H \rightarrow L)$	tPHL	4.5			12	20		25	ns
(11 - 22)		6.0				17		21	



MN74HC133/MN74HC133S

13-Input NAND Gate

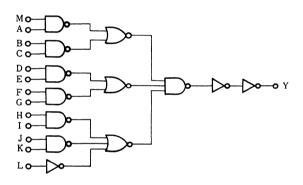
■ Description

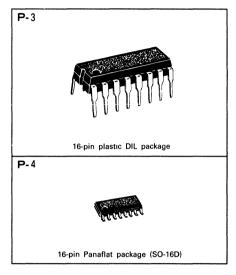
MN74HC133/MN74HC133S contain 13-input positive isolation NAND gate.

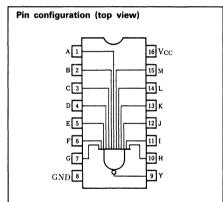
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic Diagram







■ Absolute Maximum Ratings

	Parameter	•	Symbol	Rating	Unit
Supply voltage	ge		V_{cc}	$-0.5 \sim +7.0$	V
Input/output	voltage		$V_{\rm I}, V_{\rm O}$	−0.5∼V _{CC} +0.5	V
Input protect	tion diode current		I _{IK}	±20	mA
Output paras	sitic diode current		Іок	±20	mA
Output curre	ent		Ιo	±25	mA
Supply curre	nt		I_{CC} , I_{GND}	±50	mA
Storage temp	perature range		Tstg	-65~+150	C
	MN 74 HC 133	Ta=-40~+60°C	P_{D}	400	mW
Power	MIN 14 HC 133	Ta=+60~+85°C	FD	Decrease to 200mW at the rate of 8mW/°C	111 VV
dissipation	MN74HC133S	Ta=-40~+60°C	P_{D}	275	mW
	MN74HC1333	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 3.8mW/°C	III VV

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V _i ,V _o		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		37	Те	st Condition	ons		Te	mperatur	e		
Parameter	Symbol	Vcc	17			,	Γa=25	C	Ta=-40	~+85℃	Unit
		(V)	V _I	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5	ļ	4.4		
Output HIGH voltage	VoH	6.0	or	-20.0	μA	5.9	6.0		5.9		v
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	ļ	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	VIH	20.0	μA		0.0	0.1		0.1	v
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_1	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_1 = V_C$	c or GNI	$D,I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

					Te	emperatu	re		
Parameter	Symbol	Vcc	Test Conditions		Ta=25℃	C .	Ta=-40	0~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5		ļ	8	15		19	ns
		6.0			7	13		16	
***************************************		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0				150		190	
Propagation time $(L \rightarrow H)$	tPLH	4.5			17	30		38	ns
(L / II)		6.0				26		33	
		2.0				125		155	
Propagation time $(H \rightarrow L)$	tPHL	4.5			14	25		31	ns
(11 · 22)		6.0				21		26	



MN74HC137/MN74HC137S

3-to-8 Line Decoder with Address Latches (Inverted Output)

■ Description

MN74HC137/MN74HC137S are high-speed 3-to-8 line decoders with three address latches. Addresses are stored, when $\overline{\rm GL}$ input is "H". When enable input G1 is "H" and G2 is "L", the output depending on A, B and C inputs become "L", and all other outputs become "H". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

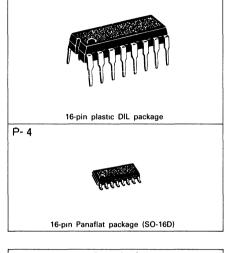
■ Truth Table

		Inp	ut						Out	put			
I	Enable	е		Select	t				Out	put			
GL	G1	$\overline{G}2$	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
×	×	Н	X	×	×	Н	Н	Н	Н	Н	Н	Н	H
×	L	×	×	×	×	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	L	Η	Н	L	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
L	Н	L	L	Н	Н	Н	Н	Н	L	Н	H	Н	Н
L	Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	H
L	Н	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
L	H	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
L	H	L	Н	Н	Н	Н	Н	H	Н	Н	Н	Н	L
Н	Н	L	×	×	×	Output corresponding to stored address L all others, H							

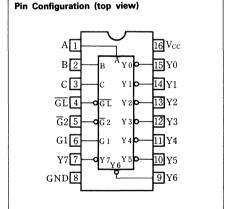
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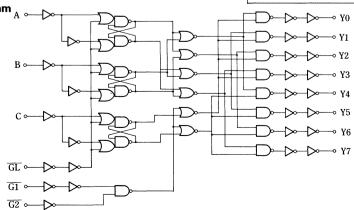
- 1. H: HIGH level
- 2. L: LOW level
- 3. ×: Either HIGH or LOW; doesn't matter





P- 3





■ Absolute Maximum Ratings

	Paramet	er	Symbol	Rating	Unit
Supply voltag	e		V _{cc}	-0.5~+7.0	V
Input/output	out/output voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protect	ion diode current		I _{IK}	±20	mA
Output parasi	itic diode current		I _{OK}	±20	mA
Output curre	nt		Io	±25	mA
Supply curren	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	erature range		Tstg	-65~+150	°C
	MN74HC137	Ta=-40~+60°C	PD	400	mW
Power	WIN74HC137	$Ta = +60 \sim +85^{\circ}C$] []	Decrease to 200mW at the rate of 8mW/°C	11144
dissipateion	MN74HC137S	Ta=-40~+60°C	PD	275	mW
	WIN /4FIC 13/5	Ta=+60~+85°C	1 1	Decrease to 200mW at the rate of 3.8mW/°C	11177

Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		$V_{CC}=2.0V$	0~1000	ns
Input rise and fall time	t _r , t _f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0	0~400	ns

■ DC Characteristics (GND=0V)

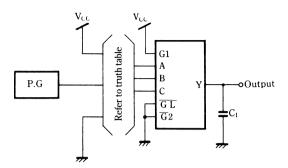
			Tes	t Condition	ons		Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	W	T			Ta=25°C		Ta=-40	~+85°C	Unit
		(1)	V _I	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	V
		2.0		-20.0	μΑ	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μΑ	4.4	4.5		4.4		V
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		V
		6.0		→5.2	mA	5.36			5.26		V
		2.0		20.0	μΑ		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μΑ		0.0	0.1		0.1	V
Output LOW voltage	V_{OL}	6.0	or	20.0	μΑ		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	II	6.0	V _I =	V _{CC} or G	ND			±0.1		±1.0	μΑ
Quiescent supply current	I_{CC}	6.0	$V_1 = V_{CC}$	or GND	$I_0=0$			8.0		80.0	μΑ



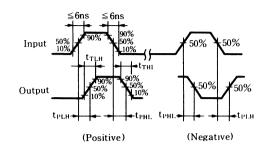
■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C_L=50pF)

					Te	emperatu	re		
Parameter	Symbol	(V)	Test Conditions		Ta=25°C		Ta = -40	~+85°C	Unit
		(')		min.	typ.	max.	min.	max.	
		2.0			23	75		95	
Output rise time	t _{TLH}	4.5			9	15		19	ns
		6.0			8	13		16	
		2.0			19	75		95	
Output fall time	t _{THL}	4.5			8	15		19	ns
		6.0			7	13		16	
Propagation time		2.0			49	150		190	
$A, B, C \rightarrow Y$	t _{PLH}	4.5	•		24	30		38	ns
(L→H)		6.0			21	26		33	
Propagation time		2.0			41	150		190	
A, B, C→Y	t _{PHL}	4.5			22	30		38	ns
(H→L)		6.0			21	26		33	
Propagation time		2.0			49	150		190	
GL→Ÿ	t _{PLH}	4.5			23	30		38	ns
(L→H)		6.0			20	26		33	
Propagation time		2.0			52	150		190	
$GL \rightarrow Y$	t _{PHL}	4.5			22	30		38	ns
(H→H)		6.0			20	26		33	
Propagation time		2.0			35	150		190	
G1→Ÿ	t _{PLH}	4.5			19	30		38	ns
(L→H)		6.0			15	26		33	
Propagation time		2.0			35	150		190	
G1→Ÿ	t _{PHL}	4.5			19	30		38	ns
$(H \rightarrow Y)$		6.0			15	26		33	
Propagation time		2.0			35	150		190	
G2→Y	t _{PLH}	4.5			18	30		38	ns
(L→H)		6.0			17	26		33	
Propagation time		2.0			35	150		190	
$\overline{G}2 \rightarrow Y$	t _{PHL}	4.5			19	30		38	ns
(H→L)		6.0			18	26		33	
		2.0			≦6	100		125	
Minimum pulse width GL→Y	t _w	4.5			≦6	20		25	ns
OD /I		6.0			≦6	17		21	
Minimum		2.0			17	100		125	
Set-up time	t _{su}	4.5			4	20		25	ns
A, B, C		6.0			2	17		21	
		2.0			_	75		95	
Minimum Hold time	t _h	4.5				15		19	ns
		6.0			_	13		16	

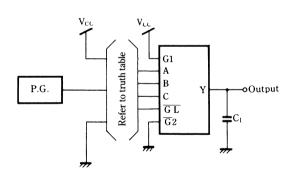
- · Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

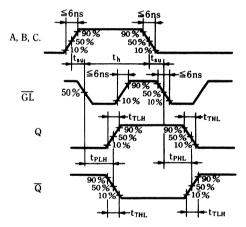


2. Waveforms



- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , t_{su} , t_{max} , t_{PLH}/t_{PHL} (CLK \rightarrow Q, \overline{Q}), t_{rem} , t_h
 - 1. Measuring Circuit (t_{PLH},t_{PHL})





MN74HC138/MN74HC138S

3-to-8 Line Decoder

■ Description

MN74HC138/MN74HC138S are high-speed 3-to-8 line decoders decoding one of eight ouput lines depending on the condition of three select inputs (A, B and C) and three enable inputs (G1, G2A and G2B)

The enable input consists of an active LOW of 2-inputs and an active HIGH of 1-input, with makes the subsidiary connection easy. Low power dissipation and high noise margin equivalent to standard CMOS; operation speed of LS TTL. LS TTL 10 inputs can be directly driven.

Resistors and diode are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

■ Truth Table

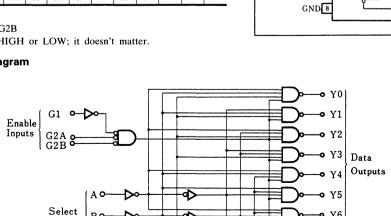
		Input	t					Out	nt			
Ena	ble	S	Selec	t				Out	.put			
G1	G2	С	В	Α	Y0	Y1	Y3	Y2	Y4	Y5	Y6	Y7
×	Н	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н
L	×	×	×	×	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

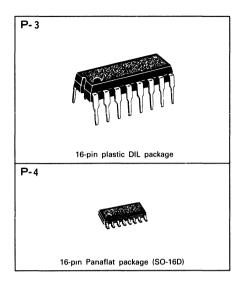
Note:

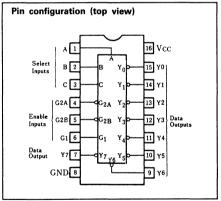
- 1. $G_2 = G2A + G2B$
- 2. ×: Either HIGH or LOW; it doesn't matter.

Inputs

■ Logic Diagram







■ Absolute Maximum Ratings

	Parameter		Symbol	Rating	Unit
Supply voltage	ge		V_{CC}	-0.5~+7.0	V
Input/output	Input/output voltage			$-0.5 \sim V_{\rm cc} + 0.5$	V
Input protect	tion diode current		I _{IK}	±20	mA
Output paras	itic diode current		Ioĸ	±20	mA
Output curre	Output current		Io	±25	mA
Supply curre	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	perature range		Tstg	−65~+150	°C
	MN74UC120	Ta=-40~+60℃	P_{D}	400	mW
Power	Power MN74HC138 $Ta=+60\sim+85$ °C		FD	Decrease to 200mW at the rate of 8mW/°C	m vv
dissipation	MN74HC138S	Ta=-40~+60℃	D-	275	mW
	WIN/40C1385	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	m w

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		$V_{\rm cc}$	Tes	st Condition	ons		T	emperatu	re		
Parameter	Symbol	(V)	Vi	Io		•	Γa=25℃	C	Ta=-40)~+85℃	Unit
		(v)	l vi	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5	1			3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86	ĺ		3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
*		4.5	VII.	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_1 = V_{C}$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CC}$	or GNI	$0, I_0=0$			8.0		80.0	μA

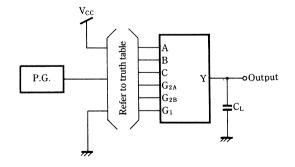


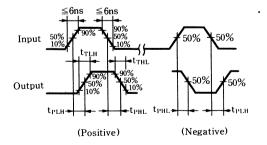
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

		.,,			Т	empera	ture		
Parameter	Symbol	Vcc	Test Conditions	,	Γa=25°	2	Ta = -4	0~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	tTHL	4.5			7	15	l	19	ns
		6.0			6	13		16	
D		2.0				200		250	
Propagation time	tPLH	4.5			22	40		50	ns
A, B, $C \rightarrow Y$ ($L \rightarrow H$)		6.0				34		43	
D		2.0				175		220	
Propagation time	tPHL	4.5			19	35		44	ns
A, B, $C \rightarrow Y (H \rightarrow L)$		6.0				30		37	
D		2.0				200		250	
Propagation time	tPLH	4.5			25	40		50	ns
Enable G1 \rightarrow Y (L \rightarrow H)		6.0				34		43	
D		2.0				175		220	
Propagation time	tPHL	4.5			20	35		44	ns
Enable G1 \rightarrow Y (H \rightarrow L)		6.0				30		37	
Propagation time		2.0	***************************************			200		250	
Enable G2 A, G2 B→Y	tPLH	4.5			22	40		50	ns
(L →H)		6.0			""	34		43	
Propagation time		2.0				175		220	
Enable G2 A, G2 B→Y	tPHL	4.5			19	35		44	ns
(H→L)		6.0			13	30		37	

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit





MN74HC139/MN74HC139S

Dual 2-to-4 Line Decoders

■ Description

MN74HC139/MN74HC139S are high-speed silicon gate CMOS, 2-to-4 line decoders decoding one of 4 output lines depending on the condition of two select inputs (A and B) and one enable input (G). Two independent 2-to-4 line decoder/demultiplexers are used on one clip.

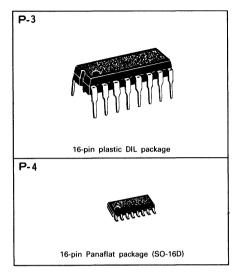
Low power dissipation and high noise margin equivalent to standard CMOS; operation speed of LS TTL. LS TTL 10 inputs can be directly driven. Are sistor and diode are provided in $V_{\rm CC}$ and GND to protect the input/out put from damage by static electricity. Same pin configuration and function as standard 54LS/74LS.

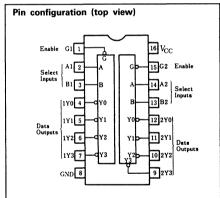
■ Truth table

-	Inpu	t			0.4		
_	Enable	Sel	ect		Outp	ut	
	G	В	A	Y ₀	Y ₁	Y ₂	Y 3
_	Н	×	×	Н	Н	Н	Н
	L	L	L	L	Н	Н	Н
	L	L	Н	Н	L	Н	Н
	L	Н	L	Н	Н	L	Н
	L	Н	Н	Н	Н	Н	L

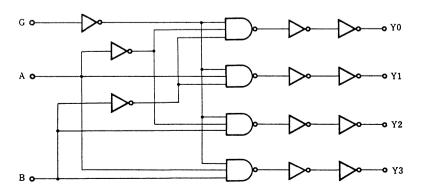
Note:

1. ×: Either HIGH or LOW; it doesn't matter





■ Logic Diagram





■ Absolute Maximum Ratings

	Parameter	•	Symbol	Rating	Unit						
Supply voltage	ge	,		•		;		:		-0.5~+7.0	V
Input/output	Input/output voltage			$-0.5 \sim V_{\rm CC} + 0.5$	V						
Input protect	ion diode current		I _{IK}	±20	mA						
Output paras	itic diode current		Іок	±20	mA						
Output curre	nt		Io	±25	mA						
Supply curre	nt		I _{CC} , I _{GND}	±50	mA						
Storage temp	oerature range		Tstg	-65~+150	${\mathbb C}$						
	MN74HC 139	Ta=-40~+60℃	P_{D}	400	mW						
Power	MN/4HC139	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 8mW/°C	III VV						
dissipation	MN74HC139S	Ta=-40~+60℃	P_{D}	275	mW						
	MN74HC1395	Ta=+60~+85℃	PD	Decrease to 200mW at the rate of 3.8mW/°C	m vv						

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm CC}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

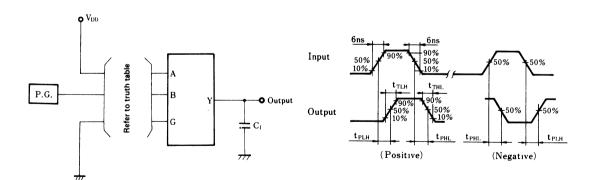
		17	Te	st Condition	ons		T	emperatu	ire		
Parameter	Symbol	Vcc	Vı	I _O		,	Γa=25 °	2	Ta=-40)~+85℃	Unit
		(V)	V _I	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μΑ	5.9	6.0	İ	5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_{i} = V_{C}$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	$I_{\rm CC}$	6.0	$V_I = V_C$	c or GN	$D, I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem \leq 6ns, C_L =50pF)

					T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta=-40	~+85°C	Unit
	:			min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0				125		155	
Propagation time A, B→Y (L→H)	t _{PLH}	4.5			13	25		31	ns
1, 2 1 (2 11)		6.0				21		26	
		2.0				100		125	
Propagation time A, $B \rightarrow Y (H \rightarrow L)$	t _{PHL}	4.5			12	20		25	ns
1, 2 / 1 (11 / 2)		6.0				17		21	
		2.0				125		155	
Propagation time Enable $G \rightarrow Y (L \rightarrow H)$	t _{PLH}	4.5			13	25		31	ns
3 · 1 (2 · 11)		6.0				21		26	
		2.0				100		125	
Propagation time Enable $G \rightarrow Y (H \rightarrow L)$	t _{PHL}	4.5			12	20		25	ns
G / 1 (11 / 11)		6.0				17		21	

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH},t_{PHL})



MN74HC147/MN74HC147S

10-to-4 Line Priority Encoder

■ Description

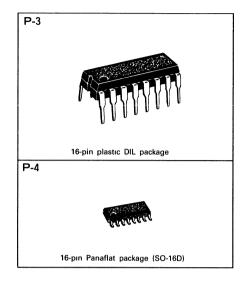
MN74HC147/MN74HC147S are 10-to-4 line priority encoders which prioritize the highest input and encode ten data lines to four data lines, when two or more input data are applied simultaneously. The binary signal 0 is encoded when all nine data inputs are "H". When all inputs and outputs are "L", the encoder is active. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

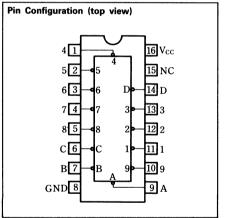
■ Truth table

					Inpu	t			Out	put			
	1	2	3	4	5	6	7	8	9	D	С	В	Α
	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
	×	×	×	×	X	×	X	×	L	L	Η	Н	L
	×	×	×	×	×	×	×	L	Н	L	Н	Н	Н
	×	×	×	×	×	×	L	Н	Н	Н	L	L	L
	×	×	×	×	×	L	Н	Н	Н	Н	L	L	Н
	×	×	×	×	L	Н	Н	Н	Н	Н	L	Н	L
	×	×	×	L	Н	Н	Н	Н	Н	Н	L	Н	H
	×	×	L	Н	Н	Н	Н	Н	Н	Н	Н	L	L
	×	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
_	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

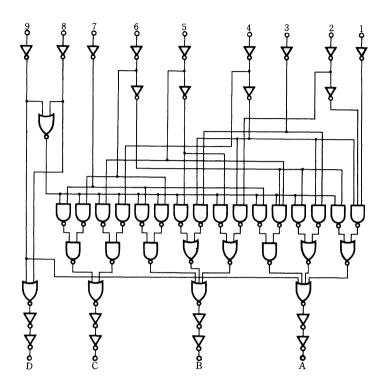
Note:

1. X: Either HIGH or LOW; it doesn't matter





■ Logic Diagram



■ Absolute Maximum Ratings

	Paramete	er	Symbol	Rating	Unit	
Supply volta	Itage		$V_{\rm cc}$	$-0.5 \sim +7.0$	V	
Input/output	voltage		V ₁ , V ₀	$-0.5 \sim V_{\rm CC} + 0.5$	V	
Input protec	tion diode current		Iıĸ	±20	mA	
Output paras	sitic diode current		Іок	±20	mA	
Output curre	ent		Io	±25	mA	
Supply curre	ent		I _{CC} , I _{GND}	±50	mA	
Storage tem	perature range		Tstg	-65∼+150	r	
	MN74 HC14 7	Ta=-40~+60℃	ъ	400	mW	
Power	MN/4HC147	Ta=+60~+85 ℃	P_D	Decrease to 200mW at the rate of 8mW/°C	III VV	
dissipation	MN74HC147S	Ta=-40~+60°C		275	mW	
	MN/4HC14/5	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C		



■ Operating Conditions

Parameter	Symbol	V _{cc} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	v
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

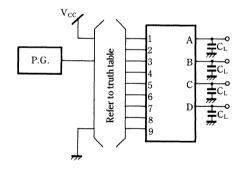
		V _{cc}	Tes	st Condition	ons		T	emperatu	ire	$ \begin{array}{c cccc} Ta = -40 \sim +85 \% \\ \hline min. & max. \\ 1.5 & & & \\ 3.15 & & & \\ 4.2 & & & \\ & & & 0.3 \\ & & & 0.9 \\ & & & 1.2 \\ \hline 1.9 & & \\ 4.4 & & \\ 5.9 & & & \\ \end{array} $	
Parameter	Symbol	(V)	Vı	Io r		,	Γa=25°	2	Ta=-40)~+85℃	Unit
		(v)	V I	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	i	4.5	V _{IH}	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μ A		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Ii	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_{\rm I} = V_{\rm CO}$	c or GNI	$I_0=0$			8.0		80.0	μA

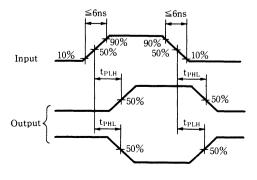
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

		17			T	emperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Γa=25°	;	$T_a = -40$	0~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	t _{TI.H}	4.5			8	15		19	ns
		6.0			7	13	ļ	16	
		2.0				75		95	
Output fall time	tthi.	4.5				15		19	ns
		6.0				13		16	
Propagation time		2.0				175		220	
$1 \sim 9 \rightarrow A$, B, C	tPLH	4.5				35	l	44	ns
$(\Gamma \rightarrow H)$		6.0				30		37	
Propagation time		2.0				175		220	
$1 \sim 9 \rightarrow A$, B, C	t PHI.	4.5				35		44	ns
$(H \rightarrow L)$		6.0				30		37	
D		2.0				125		155	
Propagation time	tPLH	4.5				25		31	ns
$1 \sim 9 \rightarrow D(L \rightarrow H)$		6.0				21		26	
D		2.0				125		155	
Propagation time	t PHI.	4.5				25		31	ns
$1 \sim 9 \rightarrow D (H \rightarrow L)$		6.0				21		26	

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH},t_{PHL})







MN74HC148/MN74HC148S

8-to-3 Line Priority Encoder

■ Description

MN74HC148/MN74HC148S are 8-to-3 line priority encoders which detect the most LOW out of eight input signals and output a binary code signal. Input consists of eight input signals (0 - 7) and an EI input. When EI input is "H", encoding stops and all outputs become "H".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Truth Table

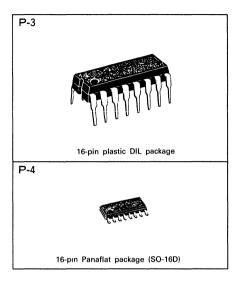
				Inpu	t					(Outpu	ıt	
ΕI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
Н	×	×	×	×	×	×	×	×	Н	Н	Н	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	×	×	×	×	×	×	×	L	L	L	L	L	Н
L	×	×	×	×	×	×	L	Н	L	L	Н	L	Н
L	×	×	×	×	×	L	Н	Н	L	Н	L	L	Н
L	×	×	×	×	L	Н	Н	Н	L	Н	Н	L	Н
L	×	×	×	L	Н	Н	Н	Н	Н	L	L	L	Н
L	×	×	L	Н	Н	Н	Н	Н	Н	L	Н	L	Н
L	×	L	Н	Н	Н	Н	Н	Н	Н	Н	L	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н

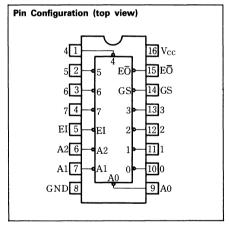
Note:

H: HIGH level

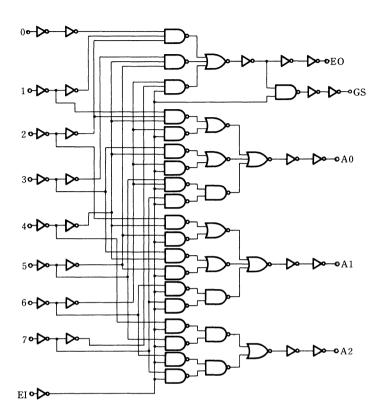
L: LOW level

×: Either HIGH or LOW; it doesn't matter





■ Logic Diagram



■ Absolute Maximum Ratings

	Parameter	-	Symbol	Rating	Unit	
Supply volta	voltage		V_{CC}	-0.5~+7.0	v	
Input/output	utput voltage		V1, Vo	$-0.5 \sim V_{\rm cc} + 0.5$	V	
Input protec	tion diode current		Iıĸ	±20	mA	
Output paras	sitic diode current		Іок	±20	mA	
Output curre	ent		Ιo	±25	mA	
Supply curre	ent	nt		±50	mA	
Storage tem	perature range		Tstg	−65∼+150	${\mathfrak C}$	
	MN74HC148	Ta=-40~+60℃	P_D	400	mW	
Power	MIN/4 II C146	Ta=+60~+85℃	Pp	Decrease to 200mW at the rate of 8mW/°C	III VV	
dissipation	MN74HC148S	Ta=-40~+60℃	D-	275	mW	
	MIN/411C1485	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	IU AA	



High-Speed CMOS Logic MN74HC Series

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V _I , V _O		0∼V _{cc}	v
Operating temperature range	TA		-40~+85	c
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

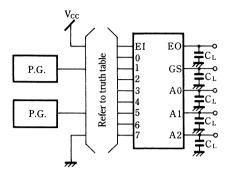
		17	Te	st Condition	ons		Те	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vı	Lo	I _o		Ta=25℃)~+85℃	Unit
		(•)	V I	10	Unit	min.	typ.	max.	min.	max.	
	-	2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5	1	4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μΑ	5.9	6.0	1	5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA		l	0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I ₁	6.0	$V_{\rm I} = V_{\rm C}$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GNI	$I_0=0$			8.0		80.0	μA

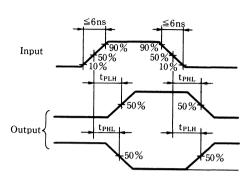
\blacksquare AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

		Temperature							
Parameter	Symbol	Vcc	Test Conditions		Γa=25°C		$T_a = -4$)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15	1	19	ns
		6.0		1	7	13	,	16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13	1	16	
Propagation time		2.0				175		220	
$0 \sim 7 \rightarrow A0$, A1, A2	tPLH	4.5				35		44	ns
(L→H)		6.0				30		37	
Propagation time		2.0				175		220	
$0 \sim 7 \rightarrow A0$, A1, A2	tPHL	4.5				35		44	ns
(H→L)		6.0				30		37	
Propagation time		2.0				175		220	
$0 \sim 7 \rightarrow EO (L \rightarrow H)$	tPLH	4.5				35		44	ns
0 -7 -EO (E -II)		6.0				30		37	
Propagation time		2.0				175		220	
0~7→EO (H→L)	tPHL	4.5				35		44	ns
0~7→EO (H→L)		6.0				30		37	
Propagation time		2.0				200		250	
	tPLH	4.5				40		50	ns
0~7→GS (L→H)		6.0				34		43	
Propagation time		2.0				200		250	
	t PHL	4.5				40		50	ns
0~7→GS (H→L)		6.0				34		43	
Propagation time		2.0				150		190	
EI → A0, A1, A2	t PLH	4.5				30		38	ns
$(\Gamma \rightarrow H)$		6.0				26		33	
Propagation time		2.0				150		190	
EI→A0, A1, A2	t PHL	4.5				30		38	ns
(H→L)		6.0				26		33	
Propagation time		2.0				175		220	
EI→GS (L→H)	tPLH	4.5				35		44	ns
EI→G5 (L→n)		6.0				30		37	
Duna anotica tima		2.0				175		220	
Propagation time EI→GS (H→L)	t _{PHL}	4.5				35		44	ns
		6.0				30		37	
Propagation time		2.0				150		190	
	tplH	4.5				30		38	ns
EI →EO (L→H)		6.0				26		33	
Proposition time		2.0				150		190	
Propagation time	tPHL	4.5				30		38	ns
$EI \rightarrow EO (H \rightarrow L)$		6.0				26		33	



- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})





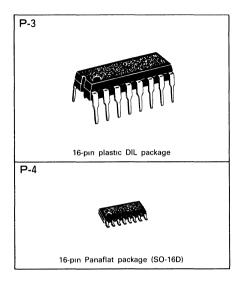
MN74HC151/MN74HC151S

8-Channel Digital Multiplexer

■ Description

MN74HC151/MN74HC151S are digital multiplexer, which selects one input from 8-channel data input according to select input (A, B C), transfer data to the reverse phase outputs W and Y mutually. When strobe input is "L", the output is selected by the select input combination. When strobe input is "H", output W is "H" and output Y is "L".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

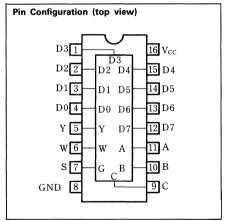


■ Truth Table

	I	nput		Ou	tput
	Select		Strobe	Y	W
С	В	A	S	Y	VV
×	×	×	Н	L	H
L	L	L	L	D0	$\overline{\mathrm{D}}\mathrm{0}$
L	L	Н	L	D1	$\overline{\mathrm{D}}$ 1
L	Н	L	L	D2	$\overline{\mathrm{D2}}$
L	Н	Н	L	D3	
Н	L	L	L	D4	$\overline{\overline{\mathrm{D4}}}$
Н	L	Н	L	D5	D5
Н	Н	L	L	D6	$\overline{\mathrm{D}6}$
Н	Н	Н	L	D7	D7

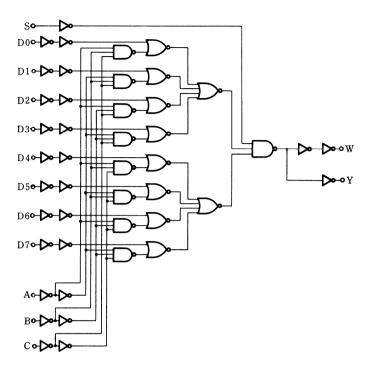
Note:

1. X: Either HIGH or LOW; it doesn't matter D0, D1, D7: respective data input level





■ Logic diagram



■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit
Supply voltage	ge		V_{CC}	-0.5~+7.0	V
Input/output	voltage		V _I ,V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protec	tion diode current		Iıĸ	±20	mA
Output paras	sitic diode current		Іок	±20	mA
Output curre	Output current			±25	mA
Supply curre	nt		I _{CC} , I _{GND}	±50	mA
Storage tem	nperature range		Tstg	-65∼+150	C
	MNZALICIEI	Ta=-40~+60℃	P_{D}	400	mW
Power	Power MN74 HC151 $Ta=+60\sim+85$ °C			Decrease to 200mW at the rate of 8mW/°C	m vv
dissipation	MN74UC151C	Ta=-40~+60℃	ъ	275	117
	MN74HC151S	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		W	Te	st Conditio	ons		Т	emperatı	ıre		
Parameter	Symbol	(V)	V ₁			Ta=25 ℃			$T_a = -40 \sim +85^{\circ}$		Unit
		,	VI	I_0	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VII	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36		1	5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{C}$	c or GNI	$0, I_0=0$			8.0		80.0	μA

\blacksquare AC Characteristics (GND=0V, Input transition time ${\leq}6ns,~C_L{=}50pF)$

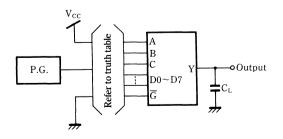
		Vcc			Ter	nperatu	re		
Parameter	Symbol	(V)	Test Conditions		$Ta = 25^{\circ}$	2	Ta = -4	0~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2. 0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	tTHL	4.5			7	15		19	ns
		6.0			6	13		16	
Propagation time		2. 0				200		250	
A, B, $C \rightarrow Y (L \rightarrow H)$	tpLH	4.5			23	40		50	ns
$A, B, C \rightarrow Y (L \rightarrow H)$		6.0				34		43	
Propagation time		2. 0				175		220	
A, B, $C \rightarrow Y (H \rightarrow L)$	tPHL	4.5			21	35		44	ns
$A, B, C \rightarrow Y (H \rightarrow L)$		6.0				30		37	
Propagation time		2.0				200		250	
A, B, $C \rightarrow W (L \rightarrow H)$	tPLH	4.5			22	40		50	ns
$A, B, C \rightarrow W (L \rightarrow H)$		6.0				34		43	
Propagation time		2. 0				200		250	
A, B, C→W (H→L)	tPHL	4.5			22	40		50	ns
$A, B, C \rightarrow W (H \rightarrow L)$		6.0				34		43	

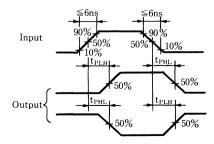


■ AC/Characteristics (Cont'd)

-		W			Ten	peratu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Γa=25°C		$T_a = -4$	0~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
Duna matica tima		2.0				100		125	
Propagation time $S \rightarrow Y (L \rightarrow H)$	t PLH	4.5			10	20		25	ns
S→1 (L→n)		6.0				17		21	
Propagation time		2.0				75		95	
S → Y (H→L)	t PHI	4.5			9	15		19	ns
3 · 1 (n→L)		6.0				13		16	
Propagation time		2.0				100		125	
• -	t PLH	4.5			12	20		25	ns
S→W (L→H)		6.0				17		21	
Duana gatean tima		2.0				100		125	
Propagation time	tPHL	4.5			10	20		25	ns
S→W (H→L)		6.0				17		21	
D		2.0				125		155	
Propagation time	tPLH	4.5			13	25		31	ns
$D \rightarrow Y (L \rightarrow H)$		6.0				21		26	
ъ:		2.0				100		125	
Propagation time	t _{PHL}	4.5			12	20		25	ns
$D \rightarrow Y (H \rightarrow L)$		6.0				17		21	
D (' ('		2.0				100		125	
Propagation time	t PLH	4.5			12	20		25	ns
$D \rightarrow W (L \rightarrow H)$		6.0				17		21	
D		2.0				100		125	
Propagation time	tPHL	4.5			12	20		25	ns
$D \rightarrow W (H \rightarrow L)$		6.0				17		21	

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})





MN74HC153/MN74HC153S

Dual 4-Input Multiplexer

■ Description

MN74HC153/MN74HC153S are dual 4-input multiplexer which transfer one of four data to output Y according to the common select input (A, B). Each multiplexer has respective enable input multiplexer functions at LOW level. At HIGH level, output is fixed LOW.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

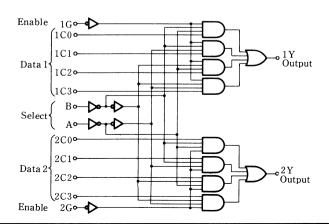
■ Truth table

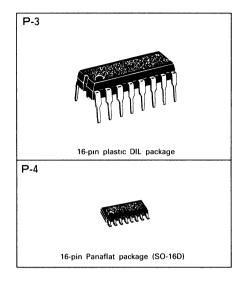
	ect uts		Data	Inputs	3	Enable	Output
В	A	C0 C1 C2 C3		G	Y		
×	×	×	×	×	×	Н	L
L	L	L	×	×	×	L	L
L	L	Н	×	×	×	L	Н
L	Н	×	L	×	×	L	L
L	Н	×	Н	×	×	L	Н
Н	L	×	×	L	×	L	L
H	L	×	×	Н	×	L	Н
Н	Н	×	×	×	L	L	L
Н	Н	×	×	×	Н	L	Н

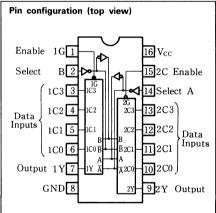
Note:

1. X: Either HIGH or LOW; it doesn't matter

■ Logic Diagram









■ Absolute Maximum Ratings

	Parameter		Symbol	Rating	Unit
Supply voltag	ge		$V_{\rm CC}$	$-0.5\!\sim\!+7.0$	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	tion diode current		I _{IK}	±20	mA
Output paras	sitic diode current		Іок	±20	mA
Output curre	Output current			±25	mA
Supply curre	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	perature range		Tstg	-65~+150	°C
	MN74 HC1 53	Ta=-40~+60℃	P_{D}	400	mW
Power	T + CO + OF CO			Decrease to 200mW at the rate of 8mW/°C	111 VV
dissipation	dissipation MN74HC153S $Ta=-40\sim+60^{\circ}$ C			275	mW
$T_a = +60 \sim +85^{\circ}$			P_D	Decrease to 200mW at the rate of 3.8mW/°C	m w

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		$1.4\!\sim\!6.0$	V
Input/output voltage	V _I ,V _O		$0 \sim V_{\rm CC}$	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

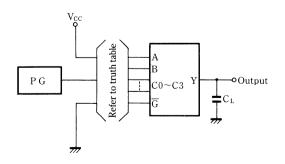
			Tes	st Conditio	ons		Te	mperatur	·e		
Parameter	Symbol	(V)	17	_		-	Γa=25°	2	Ta=-40	~+85℃	Unit
		(*)	V _I	V _I I _O	Unit	mın.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
•		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
	i	6.0		5.2	mA			0.32		0.37	
Input current	II	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	$D, I_0 = 0$			8.0		80.0	μA

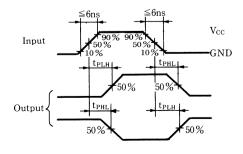
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

		.,			Te	mperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions	,	Γa=25℃	;	$T_a = -4$	0~+85℃	Unit
		()		min.	typ.	max.	mın.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	tTHL	4.5			7	15		19	ns
		6.0			6	13		16	
D		2.0			47	175		220	
Propagation time	tPLH	4.5			20	35		44	ns
$A, B \rightarrow Y (L \rightarrow H)$		6.0			17	30		37	
n		2.0			45	150		155	
Propagation time	tPHL	4.5			18	30		38	ns
$A, B \rightarrow Y (H \rightarrow L)$		6.0			14	26		26	
D		2.0			38	125		155	
Propagation time	tPLH	4.5			14	25		31	ns
$G \rightarrow Y (L \rightarrow H)$		6.0			12	21		26	
Propagation time		2.0			40	150		190	
	tPHL	4.5			17	30		38	ns
$G \rightarrow Y (H \rightarrow L)$		6.0			14	26		33	
		2.0			4 5	150		190	
Propagation time	tPLH	4.5			18	30		38	ns
$C \rightarrow Y (L \rightarrow H)$		6.0			15	26		33	
D		2.0			44	150		190	
Propagation time	tPHL	4.5			17	30		38	ns
$C \rightarrow Y (H \rightarrow L)$		6.0			14	26		33	

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})





MN74HC155/MN74HC155S

Dual 2-to-4 Line Decoders/Demultiplexers

■ Description

MN74HC155/MN74HC155S contain dual 2-bit 2-to-4 line decoders/demultiplexers.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS.

■ Truth table

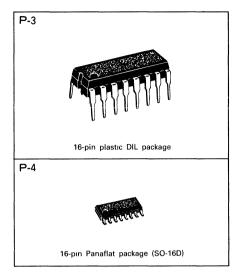
2-line to 4-line Decoder/1-line to 4-line Demultiplexer

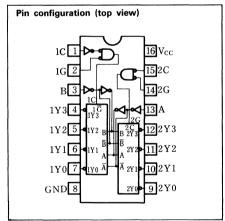
	I	nput	Output					
Sel	ect	Enable	Data	1370	1 Y 2	1 Y 2	1 Y 3	
В	A	1G	1C	1 Y 0	112	112	113	
×	×	Н	×	Н	Н	Н	Н	
L	L	L	Н	L	Н	Н	Н	
L	Н	L	Н	Н	L	Н	Н	
Н	L	L	Н	Н	Н	L	Н	
Н	H	L	Н	Н	Н	Н	L	
×	×	×	, r	Н	Н	Н	Н	

	I	nput		Out	put		
Sel	lect	Enable	Data	0370	2Y1	2 Y 2	2 Y 3
В	A	2G	2C	2Y0	211	2 1 2	213
×	×	Н	×	Н	Н	Н	Н
L	L	L	L	L	Н	Н	Н
L	Н	L	L	Н	L	Н	Н
H	L	L	L	Н	Н	L	Н
Н	Н	L	L	Н	Н	Н	L
×	×	×	Н	Н	Н	Н	Н

3-line to 8-line Decoder/1-line to 8-line Demultiplexer

Inpu	ıt	Output							
Select	Enable Data	0	1	2	3	4	5	6	7
СВА	G	2Y0	2Y1	2Y2	2Y3	1 Y 0	1 Y 1	1 Y 2	1 Y 3
$\times \times \times$	Н	Н	Н	Н	Н	Н	Н	Н	Н
L L L	L	L	Н	Н	Н	Н	Н	Н	Н
L L H	L	Н	L	Н	Н	Н	Н	Н	Н
L H L	L	Н	Н	L	Н	Н	Н	Н	Н
L H H	L	Н	Н	Н	L	Н	Н	Н	Н
H L L	L	Н	Н	Н	Н	L	Н	Н	Н
H L H	L	Н	Н	Н	Н	Н	L	Н	Н
H H L	L	Н	Н	Н	Н	Н	Н	L	Н
ннн	L	Н	Н	Н	Н	Н	Н	Н	L

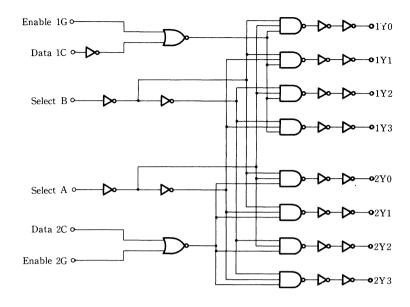




Note:

- 1. H: High level
- 2. L: Low level
- 3. X: Either H or L; it doesn't matter
- 4. C: 1C/2C inputs connected between them
- 5. G: 1G/2G inputs connected between them

■ Logic Diagram



■ Absolute Maximum Ratings

	Parameter	-	Symbol	Rating	Unit
Supply voltag	ge		V_{CC}	-0.5∼+7.0	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protect	tion diode current		I _{IK}	±20	mA
Output paras	Output parasitic diode current			±20	mA
Output curre	Output current			±25	mA
Supply curre	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	oerature range		Tstg	-65~+150	${\mathbb C}$
	MNGALIGIEE	Ta=-40~+60℃	Pp	400	mW
Power	ower MN74 HC155 $Ta=+60\sim+85$ °C		Гр	Decrease to 200mW at the rate of 8mW/°C	III VV
dissipation MN74 HC155S $Ta=-40\sim+60^{\circ}$		D.	275	mW	
$T_a = +60 \sim +85^{\circ}$			P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	III VV

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	$V_{\rm CC}$		1.4~6.0	V
Input/output voltage	V _I , V _O		$0 \sim V_{\rm CC}$	V
Operating temperature range	TA		-40~+85	°
		2.0	0~1000	ns
Input rise and fall time	t_r, t_f	4.5	0~500	ns
		6.0	0~400	ns



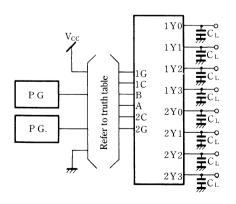
■ DC Characteristics

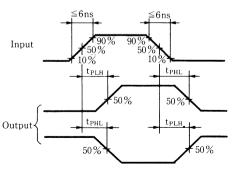
		V_{CC}	Tes	st Condition	ons		Te	mperatui	·e		
Parameter	Symbol	(V)	Vı			,	Γa=25°	2	Ta=-40)~+85°C	Unit
		(•)	Vi	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5	Į.					0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V_{IH}	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_I = V_{CO}$	or GNI	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_{\rm I} = V_{\rm C}$	c or GNI	$0,I_0=0$			8.0		80.0	μΑ

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

					Τe	mperat	ure		
Parameter	Symbol	V _{CC}	Test Conditions		Γa = 25°C	,	$T_a = -40$)~+85℃	Unit
				min.	typ.	max.	mın.	max.	
		2.0				75		95	/
Output rise time	t TLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t THL	4.5			7	15		19	ns
		6.0				13		16	
D		2.0				125		155	
Propagation time	t _{PLH}	4.5			14	25		31	ns
$A, B \rightarrow Y (L \rightarrow H)$		6.0				21		26	
Propagation time		2.0				125		155	
. ~	t _{PHL}	4.5			13	25		31	ns
$A, B \rightarrow Y (H \rightarrow L)$		6.0				21		26	
Propagation time		2.0				125		155	
1G, 2C, 2G→Y	t _{PLH}	4.5			14	25		31	ns
$(L \rightarrow H)$		6.0				21		26	
Propagation time		2.0				125		155	
1G, 2C, 2G→Y	t _{PHL}	4.5			10	25		31	ns
$(H \rightarrow \Gamma)$.		6.0				21		26	
The state of the s		2.0				125		155	
Propagation time	t _{PLH}	4.5			15	25		31	ns
$1C \rightarrow Y (L \rightarrow H)$		6.0				21		26	
		2.0				125		155	
Propagation time	t PHL	4.5			13	25		31	ns
$1C \rightarrow Y (H \rightarrow Y)$		6.0				21		26	

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})





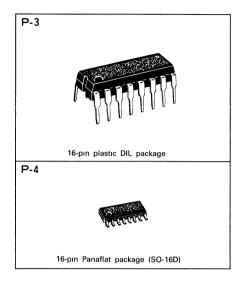
MN74HC157/MN74HC157S

Quad 2-Input Multiplexers

■ Description

MN74HC157/MN74HC157S contain quad 2-input multiplexer circuits which select one of two data. Strobe and select inputs are common to each output of the quad circuits, all outputs become "L", 1-input data is selected from each of 2-input signals depending on the state of the select input, and is transferred to quad outputs. The selected input data is transferred to output by in-phase. Adoption of a silicon date CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; and LS TTL 10-inputs can be directly driven.

Resistors and diodes are used in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



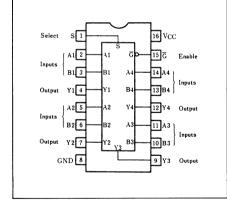
■ Truth Table

	Input									
Strobe \overline{G}	Select S	A	В	Y						
Н	× ·	×	×	L						
L	L	L	×	L						
L	L	Н	×	Н						
L	Н	×	L	L						
L	Н	×	Н	Н						

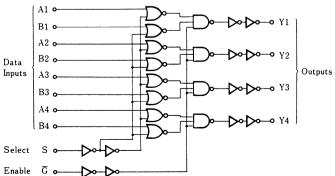
Note:

1. ×: Either HIGH or LOW; it doesn't matter

■ Logic Diagram



Pin configuration (top view)



■ Absolute Maximum Ratings

	Parameter		Symbol	Rating	Unit
Supply voltage	ge		V_{CC}	$-0.5 \sim +7.0$	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protect	on diode current		I _{IK}	±20	mA
Output paras	ıtıc diode current		Іок	±20	mA
Output curre	nt		Io	±25	mA
Supply current			I _{CC} , I _{GND}	±50	mA
Storage temperature range			Tstg	-65~+150	°C
	MN74HC157	Ta=-40~+60℃	P_{D}	400	mW
Power dissipation	WIN74HC157	Ta=+60~+85℃	ΓD	Decrease to 200mW at the rate of 8mW/°C	III VV
	MN74HC157S	Ta=-40~+60°C	D-	275	
	MN/4nC15/5	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	mW

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit	
Operating supply voltage	V_{CC}		1.4~6.0	V	
Input/output voltage	V _I , V _O		0~V _{CC}	V	
Operating temperature range	TA		-40~+85	°C	
		2.0	0~1000	ns	
Input rise and fall time	t _r , t _f	4.5	0~500	ns	
		6.0	0~400	ns	

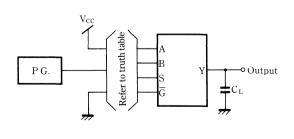
■ DC Characteristics (GND=0V)

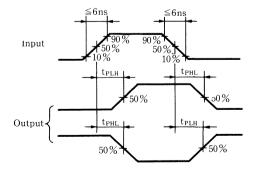
	Symbol	V _{CC} (V)	Test Conditions		Temperature						
Parameter			VI	Io Unit	Ta=25℃		Ta=-40~+85℃		Unit		
					Unit	min.	typ.	max.	min.	max.	
	Vih	2.0				1.5			1.5		
Input HIGH voltage		4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0	_	-20.0	μA	1.9	2.0		1.9		
	V _{он}	4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36		1	5.26		
	Vol	2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	II	6.0	$V_{\rm I} = V_{\rm C}$	or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	c or GN	$D, I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

	Symbol	V _{cc} (V)	Test Conditions	Temperature					
Parameter				Ta=25℃			Ta = -40~+85°C		Unit
				min.	typ.	max.	mın.	max.	
		2.0				75		95	
Output rise time	t rlh	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15		19	ns
		6.0				13		16	
D		2.0				100		125	
Propagation time	t _{PLH}	4.5			12	20		25	ns
$A, B \rightarrow Y (L \rightarrow H)$		6.0				17		21	
	t _{PHL}	2.0				100		125	
Propagation time		4.5			11	20		25	ns
$A, B \rightarrow Y (H \rightarrow L)$		6.0				17		21	
Propagation time	t _{PLH}	2.0				125		155	
		4.5			15	25		31	ns
$S \rightarrow Y (L \rightarrow H)$		6.0				21		26	
Propagation time	t _{PHL}	2.0				125		155	
		4.5			14	25		31	ns
$S \rightarrow Y (H \rightarrow L)$		6.0				21		26	
D		2.0				125		125	
Propagation time	${ m t_{PLH}}$	4.5			13	25		25	ns
$\overline{G} \rightarrow Y (L \rightarrow H)$		6.0				17		21	
p		2.0				100		125	
Propagation time	t _{PHL}	4.5			13	20		25	ns
$\overline{G} \rightarrow Y (H \rightarrow L)$		6.0				17		21	

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Cırcuit (t_{PLH}, t_{PHL})



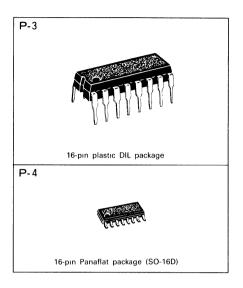


MN74HC158/MN74HC158S

Quad 2-Input Multiplexers (Inverted Output)

■ Description

MN74HC158/MN74HC158S contain quad 2-input multiplexer circuits which select one of two data. Strobe and select input is common, and, when it is "H", all output become "H". When strobe input is "L", 1-input data is selected from each of 2-input signals depending on the state of the select input, and is transferred to each of the quad outputs. Then, the selected input data is transferred to output inverted. Adoption of a silicon date CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; LS TTL 10-inputs can be directly driven. Resistors and diodes are used in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



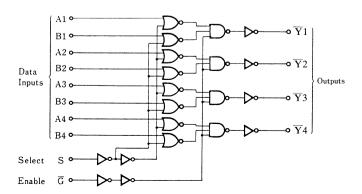
■ Truth Table

	Output			
Strobe $\overline{\mathbb{G}}$	Select S	A	В	Y
Н	×	×	×	Н
L	L	L	×	Н
L	L	Н	×	L
L	Н	×	L	Н
L	Н	×	Н	L

Note

1 × Either HIGH or LOW, it doesn't matter

■ Logic Diagram





■ Absolute Maximum Ratings

	Parameter	-	Symbol	Rating	Unit		
Supply voltag	ge		$V_{\rm cc}$	-0.5~+7.0	V		
Input/output	put voltage		tput voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protect	ion diode current		I _{IK}	±20	mA		
Output paras	itic diode current		Іок	±20	mA		
Output curre	Output current			±25	mA		
Supply curre	nt		I _{CC} , I _{GND}	±50	mA		
Storage temp	oerature range	ture range		−65~+150	$^{\circ}$		
	MN74HC158	Ta=-40~+60℃	P_{D}	400	mW		
Power	MN74HC136	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 8mW/°C	111 VV		
dissipation	MN74HC158S	Ta=-40~+60℃	D-	275	mW		
	MN/40C138S	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	III VV		

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

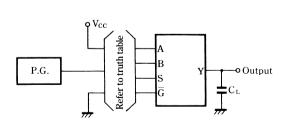
			Tes	st Conditio	ns		T	emperatu	ire		
Parameter	Symbol	V _{CC} (V)	Vı	Io ,			Γa=25°	<u> </u>	Ta=-40)~+85°C	Unit
		(•)	V _I	10	Unit	mın.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	$V_{\rm IL}$	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μ A		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μΑ	l	0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V_C$	c or GNI	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GNI	$0, I_0=0$			8.0		80.0	μA

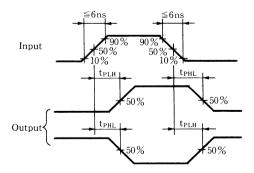
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

					T	emperat	ure		
Parameter	Symbol	Vcc	Test Conditions		Γa = 25°C	;	Ta = -40)~+85℃	Unit
		(V)		min.	typ.	max.	mın.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
Dropogotion tons		2.0				100		125	
Propagation time A, $B \rightarrow \overline{Y} (L \rightarrow H)$ t_{PLH}	4.5			11	20		25	ns	
		6.0				17		21	
D		2.0				100		125	
Propagation time A, $B \rightarrow \overline{Y}(H \rightarrow L)$	t _{PHL}	4.5			11	20		25	ns
A, B 1 (H L)		6.0				17	-	21	
Propagation time		2.0				125		155	
S $\rightarrow \overline{Y}$ (L \rightarrow H)	t _{PLH}	4.5			13	25		31	ns
5→1 (L→n)		6.0				21		26	
Propagation time		2.0				100		125	
Fropagation time $S \rightarrow \overline{Y} (H \rightarrow L)$	t _{PHL}	4.5			11	20		25	ns
5→ I (H→L)		6.0				17		21	
D		2.0				125		155	
$\begin{array}{c} \text{Propagation time} \\ \overline{G} \! \to \! \overline{Y} \; (L \! \to \! H) \end{array} \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad \qquad $	t _{PLH}	4.5			14	25		31	ns
		6.0				21		26	
D		2.0				125		155	
Propagation time $\overline{G} \rightarrow \overline{Y} (H \rightarrow L)$	t _{PHI.}	4.5			14	25		31	ns
G→Y (H→L)		6.0				21		26	

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

2. Waveforms





MN74HC160/MN74HC160S

Synchronous Decade Counter with Asynchronous Clear

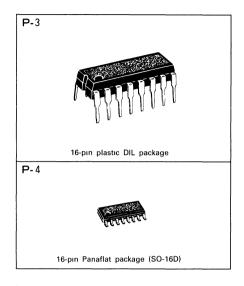
■ Description

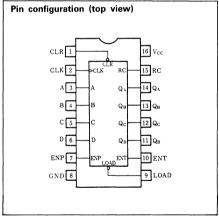
MN74HC160/MN74HC160S are pre-settable synchronous decade counters with an internal carry-look-ahead system which makes possible high-speed counter applications. Outputs of all flip-flop change at the rising edge of clock input. Since this counter is perfectly programmable, the output can be preset to both "H" and "L" by using load input. Four flip-flops are preset synchronously with the rising edge of clock input. When load input is "L", the counter stops its function, and the data corresponding with input data to be set at next clock pulse, regardless of the enable input level, appears in the output. Even if the load input becomes "H" before the rising edge of clock input, the counter doesn't operate. Clear operates asynchronously, and, when clear input is "L", it operates regardless of load or enable input level.

The carry-look-ahead circuit is used for cascade connection of an n bit synchronous counter without additional components. These junctions are performed by the enable input (ENP·ENT) of two active "HIGH" and ripple-carry (RC) outputs. When both enable inputs P and T are "H", the count can be enabled.

Ripple-carry output becomes almost the same width as output \overline{Q}_A "H".

This "H" overflow ripple-carry pulse is used to enable each connected stage to cascade. Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL. Resistors and diodes are used in the V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.





■ Truth Table

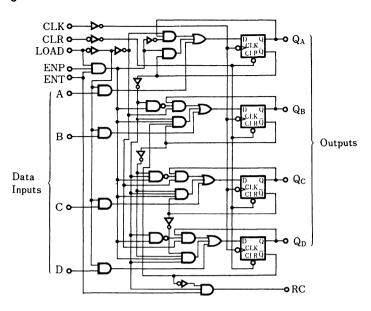
CLK	CLR	ENP	ENT	LOAD	Output
×	L	×	×	×	Clear
×	Н	Н	L	Н	Count & RC disabled
×	Н	L	Н	Н	Count disabled
×	Н	L	L	Н	Count & RC disabled
f	Н	×	×	L	Load
5	Н	Н	Н	Н	Increment Counter

Note:

1. \(\int \) When clock rises from LOW to HIGH, output increments and counts. When the load is LOW, input data is loaded.

2. ×: Either HIGH or LOW; it doesn't matter.

■ Logic Diagram



■ Absolute Maximum Ratings

	Parameter	-	Symbol	Rating	Unit
Supply voltag	y voltage		$V_{\rm CC}$	-0.5~+7.0	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	tion diode current		I _{IK}	±20	mA
Output paras	sitic diode current		Іок	±20	mΑ
Output curre	ent		Io	±25	mA
Supply curre	ent		I _{CC} , I _{GND}	±50	mA
Storage temp	temperature range		Tstg	-65~+150	${\mathfrak C}$
	MN74HC160	Ta=-40~+60℃	D.	400	mW
Power $Ta=+60\sim+85^{\circ}$		Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 8mW/°C	m vv
dissipation	MN74HC160S	Ta=-40~+60℃	D-	275	mW
	MIN/4HC160S	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	m vv

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	v
Operating temperature range	TA		-40~+85	r
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns



■ DC Characteristics (GND=0V)

		V_{CC}	Te	st Condition	ons		Т	`emperat	ure		
Parameter	Symbol	(V)	Vı	Io		,	Γa=25°	2	Ta=-40)~+85℃	Unit
		(•)	VI	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2	}		4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	Vih	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V _{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_{\rm I} = V_{\rm C}$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_i = V_{CO}$	or GN	D, $I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

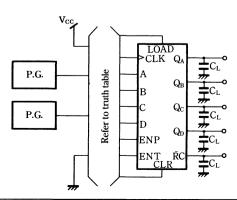
					Te	mperatu	ıre		
Parameter	Symbol	Vcc	Test Conditions	Ta	=25℃		$T_a = -40$	~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	t_{TLH}	4.5		1	8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t_{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
Propagation time		2.0				175		220	
CLK \rightarrow Q _A \sim Q _D (L \rightarrow H)	$t_{\rm PLH}$	4.5			18	35		44	ns
$CLN \rightarrow Q_A \sim Q_D (L \rightarrow H)$		6.0				30		37	
Propagation time		2.0				175		220	
	$t_{ m PHL}$	4.5			18	35		44	ns
$CLK \rightarrow Q_A \sim Q_D \ (H \rightarrow L)$		6.0				30		37	
Propagation time		2.0				175		220	
Propagation time	t _{PLH}	4.5			18	35		44	ns
CLK→RC (L→H)		6.0				30		37	
D		2.0				175		220	
Propagation time	t _{PHL}	4.5			17	35		44	ns
CLK→RC (H→L)		6.0				30		37	

■ AC Characteristics (Cont'd)

					Те	mperati	ıre		
Parameter	Symbol	V _{CC}	Test Conditions		Γa=25°C		$T_a = -40$	~+85°C	Unit
		(v)		min.	typ.	max.	min.	max.	
Propagation time		2.0				125		155	
ENT→RC (L→H)	t _{PLH}	4.5			11	25		31	ns
ENT—RC (L—II)		6.0				21		26	
Propagation time		2.0				125		155	
ENT→RC (H→L)	t _{PHL}	4.5			13	25		31	ns
ENI→RC (H→L)		6.0				21		26	
Propagation time		2.0				175		220	
	tPHL	4.5			17	35		44	ns
$CLR \rightarrow Q_A \sim Q_D (H \rightarrow L)$		6.0			Ì	30	1	37	
Propagation time		2.0				175		220	
CLR→RC (H→L)	t _{PHL}	4.5			20	35		44	ns
CLR→RC (H→L)		6.0				30		37	
Minimum Set-up time		2.0				100		125	
LOAD	tsu	4.5			9	20	1	25	ns
LOAD		6.0				17	İ	21	
Minimus Catalana		2.0				100		125	
Minimum Set-up time	tsu	4.5			5	20		25	ns
A, B, C, D		6.0			1	17		21	
		2.0			_	0		0	
Minimum Hold time	tь	4.5			-	0	ĺ	0	ns
		6.0			-	0	Ì	0	
		2.0				100		125	
Minimum pulse width	t _w	4.5		ĺ	7	20	-	25	ns
CLR		6.0				17		21	
		2.0	Por grande in the control of the con			75		95	
Minimum recovery time	trem	4.5			2	15		19	ns
		6.0				13		16	
		2.0		6			4		
Maximum clock frequency	f max	4.5		30	71		24		MHz
		6.0		35			28		

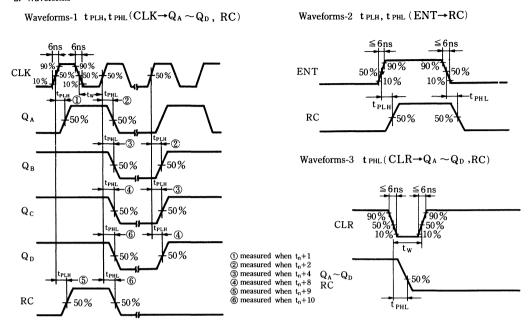
• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit

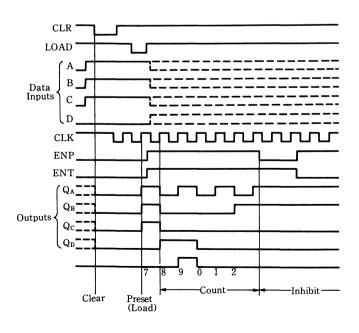




2. Waveforms



■ Timing chart



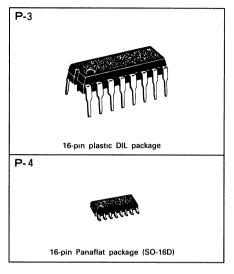
MN74HC161/MN74HC161S

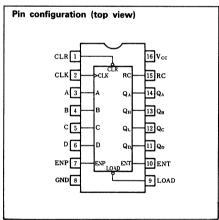
Synchronous Binary Counter

■ Description

MN74HC161/MN74HC161S are presettable synchronous binary counters with an internal carry-look-ahead system which makes possible high-speed counter applications. Outputs of all flip-flops change at the rising edge of the clock input. Since this counter is perfectly programmable, the output can be preset to both "H" and "L" by utilizing the load input. Four flip-flops are preset synchronously with the rising edge of the clock input. When the load input is "L", the counter stops its function, and the data corresponding with input data to be set at the next clock pulse, regardless of the enable input level, appears in the output. Even if the load input becomes "H" before the rising edge of clock input, the counter doesn't operate. The clear function operates asynchronously, and, when clear input is "L", it operates regardless of load or enable input level. The carry-look-ahead circuit is used for cascade connection of an n bit synchronous counter without any additional components. These functions are performed by the enable input (ENP·ENT) of two active "HIGH" and ripple-carry (RC) outputs. When both enable inputs P and T are "H", the counter can be enabled. Ripple-carry-out becomes almost the same width as output \overline{Q}_A "H".

This "H" overflow ripple-carry pulse is used to enable each stage connected to cascade. Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance and an operation speed equivalent to LS TTL. Resistors and diodes are used in the $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.





■ Truth Table

CLK	CLR	ENP	ENT	LOAD	Output
×	L	×	×	×	Clear
×	Н	Н	L	Н	Count & RC disabled
×	Н	L	Н	Н	Count disabled
×	Н	L	L	Н	Count & RC disabled
f	Н	×	×	L	Load
	Н	Н	Н	Н	Increment Counter

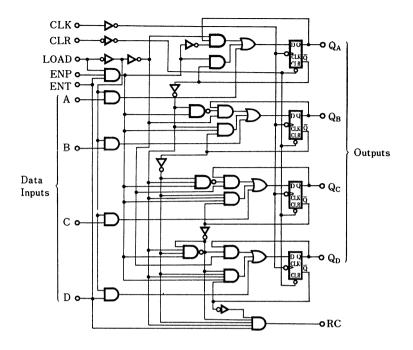
Note:

1. f: When clock rises from LOW to HIGH, output increments and counts. When the load is LOW, input data is loaded.

2. x: Either HIGH or LOW; it doesn't matter.



■ Logic Diagram



■ Absolute Maximum Ratings

	Parameter		Symbol	Rating	Unit				
Supply voltage	nge		voltage		voltage		$V_{\rm cc}$	-0.5∼+7.0	v
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm cc} + 0.5$	v				
Input protect	tion diode current		I _{IK}	±20	mA				
Output paras	sitic diode current		Іок	±20	mA				
Output curre	ent		Io	±25	mA				
Supply curre	nt		I _{CC} , I _{GND}	±50	mA				
Storage tem	perature range		Tstg	−65∼+150	С				
	MN74HC161	Ta=-40~+60℃	P_{D}	400	mW				
Power $Ta=+60\sim+85^{\circ}$			l rb	Decrease to 200mW at the rate of 8mW/°C	mvv				
dissipation	MN74HC 161S	Ta=-40~+60°C	Pp	275	mW				
	MN/4HC 1615	Ta=+60~+85℃	l PD	Decrease to 200mW at the rate of 3.8mW/°C	m vv				

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	v
Operating temperature range	TA		-40~+85	r
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

Panasonic -150-

■ DC Characteristics (GND=0V)

			Te	st Condition	ons		T	emperatu	ire		
Parameter	Symbol	V _{CC} (V)	v	,			Γa=25°	2	Ta=-40)~+85℃	Unit
		(v)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5	i			3.15		ŀ	3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
		4.5	VIH	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	VoH	6.0	or	-20.0	μ A	5.9	6.0		5.9	ĺ	V
		4.5	VIL	-4.0	mA	3.86		ļ	3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μ A		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I = V_C$	c or GNI)			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	c or GNI	$I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

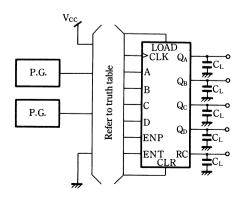
		τ,			Te	mperat	ure		
Parameter	Symbol	(V)	Test Conditions	Ta	=25℃		$T_s = -40$	~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	$\mathbf{t}_{\mathrm{TLH}}$	4.5			8	15	ļ	19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t_{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
Propagation time		2.0				150		190	
CLK \rightarrow Q _A \sim Q _D (L \rightarrow H)	t _{PLH}	4.5			18	30		38	ns
CLK-WA~WD (L-H)		6.0				26		33	
Propagation time		2.0				150		190	
CLK \rightarrow Q _A \sim Q _D (H \rightarrow L)	$\mathbf{t}_{\mathrm{PHL}}$	4.5			18	30	,	38	ns
CLK-QA~QD (H-L)		6.0				26		33	
Duran a matrica a time a		2.0				175		220	
Propagation time CLK→RC (L→H)	t_{PLH}	4.5			17	35		44	ns
CLK→RC (L→H)		6.0			,	30	j	37	
D		2.0				175		220	
Propagation time	$t_{ m PHL}$	4.5			16	35		44	ns
CLK→RC (H→L)		6.0				30		37	



■ AC Characteristics (Cont'd)

					Tei	mperatu	ıre		
Parameter	Symbol	Vcc	Test Conditions	7	Γa=25℃		Ta = -40	~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
Propagation time		2.0				100		125	
ENT→RC (L→H)	t _{PLH}	4.5			12	20		25	ns
ENI→RC(L→H)		6.0				17		21	
Propagation time		2.0				125		155	
ENT→RC (H→L)	$\mathbf{t}_{\mathrm{PHL}}$	4.5			14	25		31	ns
ENI→RC (H→L)		6.0				21		26	
D		2.0				150		190	
Propagation time	t_{PHL}	4.5			16	30		38	ns
$CLR \rightarrow Q_A \sim Q_D (H \rightarrow L)$		6.0				26		33	
Propagation time		2.0				175		220	
• 0	$t_{ m PHL}$	4.5			20	35		44	ns
$CLR \rightarrow RC (H \rightarrow L)$		6.0				30		37	
Minimum Set-up time		2.0				100		125	
LOAD	tsu	4.5			10	20		25	ns
LOAD		6.0				17		21	
Maria Cara di		2.0				100		125	
Minimum Set-up time	tsu	4.5			5	20		25	ns
A, B, C, D		6.0				17		21	
		2.0			_	0		0	
Minimum Hold time	th	4.5			_	0		0	ns
		6.0				0		0	
B.61. 1 11.1		2.0				100		125	,
Minimum pulse width	t _w	4.5			7	20		25	ns
CLK		6.0				17		21	
		2.0				75		95	
Minimum recovery time	trem	4.5			3	15		19	ns
		6.0				13		16	
		2.0		6			4		- William
Maximum clock frequency	f max	4.5		28	45		22		MHz
		6.0		33			26		

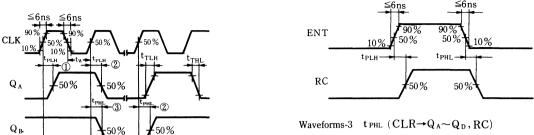
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit



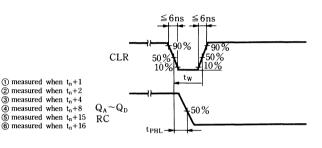
2. Waveforms

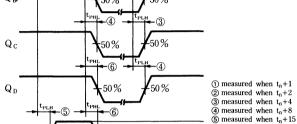
Waveforms-1 t_{PLH} , t_{PHL} (CLK $\rightarrow Q_A \sim Q_D$, RC)

Waveforms-2 t_{PLH} , t_{PHL} (ENT \rightarrow RC)



Waveforms-3 t_{PHL} (CLR $\rightarrow Q_A \sim Q_D, RC$)

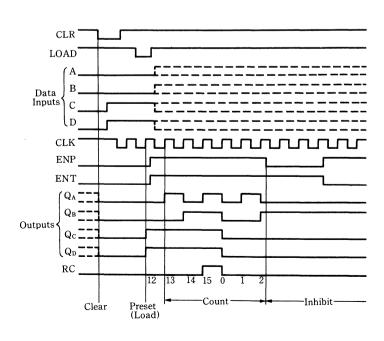




50%

■ Timing chart

RC



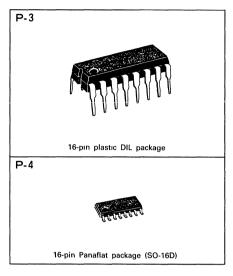
MN74HC162/MN74HC162S

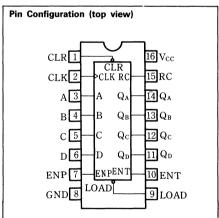
Synchronous Decade Counter with Synchronous Clear

■ Description

MN74HC162/MN74HC162S are presettable synchronous decade counters with an internal carry-look-ahead system which makes possible high-speed counter applications. Outputs of all flip-flops change at the rising edge of the clock input. Since this counter is perfectly programmable, the output can be preset to both "H" and "L" by utilizing the load input. Four flip-flops are preset synchronously with the rising edge of the clock input. When the load input is "L", the counter stops its function, and the data corresponding with input data to be set at the next clock pulse, regardless of the enable input level, appears in the output. Even if the load input becomes "H" before the rising edge of clock input, the counter doesn't operate. The clear function operates with clock synchronously, and, when clear input is "L", it operates on the rising edge of clock input. The carry-look-ahead circuit is used for cascade connection of an n bit synchronous counter without any additional components. These functions are performed by the enable input (ENP-ENT) of two active "HIGH" and ripple-carry (RC) outputs. When both enable inputs P and T are "H", the counter can be enabled. Ripple-carry-out becomes almost the same width as output \overline{Q}_A "H".

This "H" overflow ripple-carry pulse is used to enable each stage connected to cascade. Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance and an operation speed equivalent to LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are used in the $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.





■ Truth Table

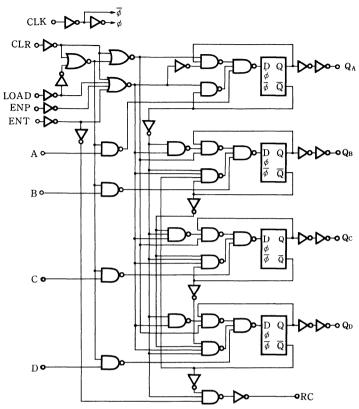
CLK	CLR	ENP	ENT	LOAD	Output
5	L	×	×	×	Clear
×	Н	Н	L	Н	Count & RC disabled
×	Н	L	Н	Н	Count disabled
×	Н	L	L	Н	Count & RC disabled
£	Н	×	×	L	Load
-5	Н	Н	Н	Н	Increment Counter

Note:

1. ____: When clock rises from LOW to HIGH, output increments and counts. When the load is LOW, input data is loaded.

2. × : Either HIGH or LOW; it doesn't matter

■ Logic Diagram



■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit				
Supply volta	oltage		y voltage		ply voltage		Vcc	-0.5~+7.0	V
Input/output	voltage		V _I ,V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V				
Input protec	tion diode current		I _{IK}	±20	mA				
Output paras	sitic diode current		Іок	±20 ·	mA				
Output current			Ιo	±25	mA				
Supply curre	ent		I _{CC} ,I _{GND}	±50	mA				
Storage tem	perature range		Tstg	-65∼+150	${\mathbb C}$				
	MN74HC162	Ta=-40~+60℃	Ъ	400	mW				
Power $Ta=+60\sim+85^{\circ}$			P_D	Decrease to 200mW at the rate of 8mW/°C	m vv				
dissipation	·		ъ	275	11/				
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$			P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW				

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	$V_{\rm I}, V_{\rm O}$		0~V _{cc}	V
Operating temperature range	T _A		-40~+85	c
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns



■ DC Characteristics (GND=0V)

		37	Те	st Condition	ons		T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vi	т			Ta=25°	C	Ta=-40)~+85℃	Unit
		(•)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{II}	4.5						0.9		0.9	V
		6.0						1.2	ĺ	1.2	
-		2.0		-20.0	μA	1.9	2.0		1.9		
	Von	4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
:		4.5	VIL	-4.0	mA	3.86)	3.76		
		6.0		-5.2	mÆ	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V _{II} .	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_1 = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_{\rm I} = V_{\rm C}$	c or GNI	D, $I_0=0$			8.0		80.0	μΑ

\blacksquare AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

		w			Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Γa= 25°	С	Ta=-40~+85 ℃		Unit
		(, ,		min.	typ.	max.	min.	max.	
		2.0	`		25	75		95	
Output rise time	t TLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15		19	ns
		6.0				13		16	
P. D.		2.0				175		220	
E Propagation time	t PLH	4.5	LOAD="H"		19	35		44	ns
$CLK \rightarrow Q_A \sim Q_D (L \rightarrow H)$		6.0				30		37	
E. Duna anation time		2.0				175		220	
E Propagation time	t PHL	4.5	LOAD="H"		18	35		44	ns
$CLK \rightarrow Q_A \sim Q_D(H \rightarrow L)$		6.0				30		37	
E Dono antion time		2.0				175		220	
E Propagation time	t PLH	4.5	LOAD="L"		19	35		44	ns
$CLK \rightarrow Q_A \sim Q_D(L \rightarrow H)$		6.0				30		37	
E Propagation time		2.0				175		220	
	t PHL	4.5	LOAD="L"		18	35		44	ns
$CLK \rightarrow Q_A \sim Q_D(H \rightarrow L)$		6.0				30		37	

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

		17			Temper	ature C	ondition		
Parameter	Symbol	V _{cc} (V)	Test Conditions	,	Ta=25°	;	Ta=-40	~+85°C	Unit
		(*)		min.	typ.	max.	min.	max.	
E Propagation time		2.0				200		250	
CLK→RC (L→H)	t PLH	4.5			25	40		50	ns
——————————————————————————————————————		6.0				34		43	
E Propagation time		2.0				200	,	250	
CLK→RC (H→L)	t PHL	4.5			23	40		50	ns
		6.0				34		43	
E Propagation time		2.0				150		190	
ENT→RC (L→H)	t PLH	4.5			15	30		38	ns
ENT-RC(L-H)		6.0				26		33	
E Propagation time		2.0				175		220	
ENT→RC (H→L)	t PHL	4.5			17	35		44	ns
ENITIC (HTL)		6.0				30		37	
		2.0				125		155	
Minimum Set-up time	t _{su}	4.5			13	25		31	ns
LOAD		6.0				21		26	
,		2.0	<u> </u>			100		125	
Minimum Set-up time	tsu	4.5			6	20		25	ns
A, B, C, D		6.0				17		21	
		2.0				125		155	
Minimum Set-up time	tsu	4.5			13	25		31	ns
CLR		6.0				21		26	
		2.0			_	0		0	
Minimum Hold time	t _h	4.5			_	0		0	ns
		6.0			_	0		0	
		2.0				100		125	
Minimum pulse width	tw	4.5			11	20		25	ns
CLK		6.0				17		21	
		2.0				125		155	
Minimum recovery time	t _{rem}	4.5			15	25		31	ns
		6.0				21		26	
		2.0		6			5		
Maximum clock frequency	f max	4.5		30	56		24		MHz
nequency		6.0		35			28		

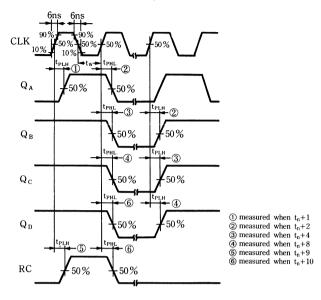


- · Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

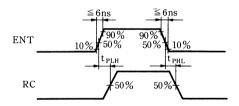
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2. Waveforms

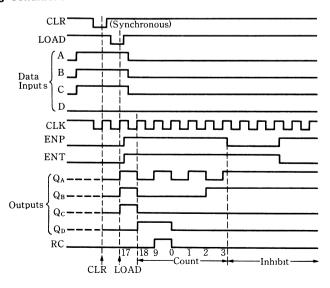
Waveforms-1 t PLH, t PHL ($CLK \rightarrow Q_A \sim Q_D$, RC)



Waveforms-2 tplH, tpHL (ENT→RC)



■ Typical Operating Conditions



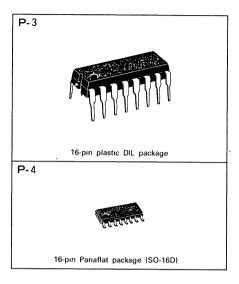
MN74HC163/MN74HC163S

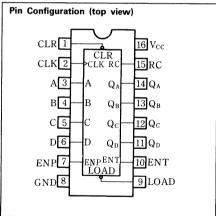
Synchronous Binary Counter with Synchronous Clear

■ Description

MN74HC163/MN74HC163S are presettable synchronous binary counters with an internal carry-look-ahead system which makes possible high-speed counter applications. Outputs of all flip-flops change at the rising edge of the clock input. Since this counter is perfectly programmable, the output can be preset to both "H" and "L" by utilizing the load input. Four flip-flops are preset synchronously with the rising edge of the clock input. When the load input is "L", the counter stops its function, and the data corresponding with input data to be set at the next clock pulse, regardless of the enable input level, appears in the output. Even if the load input becomes "H" before the rising edge of clock input, the counter doesn't operate. The clear function operates with clock synchronously, and, when clear input is "L", it operates on the rising edge of clock input. The carry-look-ahead circuit is used for cascade connection of an n bit syschronous counter without any additional components. These functions are performed by the enable input (ENP-ENT) of two active "HIGH" and ripple-carry (RC) outputs. When both enable inputs P and T are "H", the counter can be enabled. Ripple-carry-out becomes almost the same width as output \overline{Q}_A "H".

This "H" overflow ripple-carry pulse is used to enable each stage connected to cascade. Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance and an operation speed equivalent to LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are used in the $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.





■ Truth Table

CLK	CLR	ENP	ENT	LOAD	Output
5	L	×	×	×	Clear
×	Н	Н	L	Н	Count & RC disabled
×	Н	L	Н	Н	Count disabled
×	Н	L	L	Н	Count & RC disabled
f	Н	×	×	L	Load
	Н	Н	Н	Н	Increment Counter

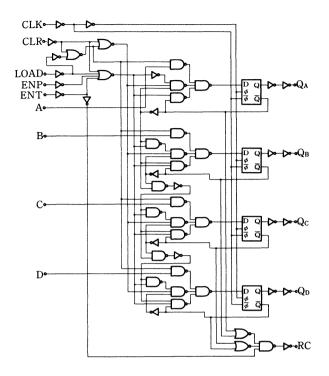
Note:

 When clock rises from LOW to HIGH, output increments and counts. When the load is LOW, input data is loaded.

2. ×: Either HIGH or LOW, it doesn't matter



■ Logic Diagram



■ Absolute Maximum Ratings

	Parameter		Symbol	Rating	Unit								
Supply voltage	oltage		oltage		voltage		voltage		ly voltage		$V_{\rm cc}$	-0.5~+7.0	V
Input/output	voltage		V_l, V_O	$-0.5 \sim V_{\rm cc} + 0.5$	V								
Input protect	ion diode current		I _{IK}	±20	mA								
Output paras	itic diode current		Iok	±20	mA								
Output curre	Output current			put current		Io	±25	mA					
Supply curre	nt		I _{CC} , I _{GND}	±50	mA								
Storage temp	oerature range		Tstg	−65∼+150	c								
	MN74HC163	Ta=-40~+60℃	P_{D}	400	mW								
Power	70 100 1050			Decrease to 200mW at the rate of 8mW/°C	III VV								
dissipation	dissipation MN74HC163S $Ta=-40\sim+60^{\circ}$			275	mW								
	$T_{a}=+60\sim+85$ °C			Decrease to 200mW at the rate of 3.8mW/°C	m vv								

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	$V_{\rm CC}$		1.4~6.0	V
Input/output voltage	V _I ,V _O		$0 \sim V_{\rm CC}$	V
Operating temperature range	T_{A}		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		17	Te	st Condition	ons		Т	`emperat	ure		
Parameter	Symbol	Vcc	v	Io		7	Γa=25°	2	Ta=-40	~+85℃	Unit
		(V)	VI	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	_
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{1L}	-4.0	mA	3.86		1	3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μΑ		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μΑ
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	c or GNI	D, $I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

		Vcc			T	emperat	ture		
Parameter	Symbol	(V)	Test Conditions	-	Γa= 25 °	C	Ta=-40)~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	tTHL	4.5			7	15		19	ns
		6.0			6	13		16	
E. Deconomista time		2.0				150		190	
E Propagation time $CLK \rightarrow Q_A \sim Q_D (L \rightarrow H)$	tPLH	4.5	LOAD= "H"		16	30		38	ns
$CLN \rightarrow Q_A \sim Q_D (L \rightarrow H)$		6.0				26		33	
E. Duono antino timo		2.0				125		155	
E Propagation time	t PHL	4.5	LOAD= "H"		15	25		31	ns
$CLK \rightarrow Q_A \sim Q_D(H \rightarrow L)$		6.0				21		26	
P. D.		2.0				150		190	
E Propagation time	t PLH	4.5	LOAD= "L"		16	30		38	ns
$CLK \rightarrow Q_A \sim Q_D (L \rightarrow H)$		6.0				26		33	
P. Donoroston dia		2.0				125		155	
E Propagation time	t PHL	4.5	LOAD= "L"		15	25		31	ns
$CLK \rightarrow Q_A \sim Q_D(H \rightarrow L)$		6.0				21		26	

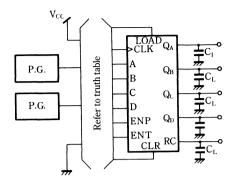


 \blacksquare AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

	V _{cc}				Temper	ature C	ondition		
Parameter	Symbol	Vcc (V)	Test Conditions	,	Ta=25 °C	2	Ta=-40)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
F.D		2.0				200		250	
E Propagation time	tPLH	4.5			24	40		50	ns
CLK→RC (L→H)		6.0				34		43	
E. Duona action time		2.0				175		220	
E Propagation time	t _{PHL}	4.5			20	35		44	ns
CLK→RC (H→L)		6.0				30		37	
B.B		2.0				125		155	
E Propagation time	t _{PLH}	4.5			14	25		31	ns
$ENT \rightarrow RC (L \rightarrow H)$		6.0				21		26	
7. P		2.0				150		190	
E Propagation time	tPHL	4.5			16	30		38	ns
ENT→RC (H→L)		6.0				26		33	
		2.0				100		125	
Minimum Set-up time	t su	4.5			12	20		25	ns
LOAD		6.0				17		21	
	y	2.0				100		125	
Minimum Set-up time	t su	4.5		}	6	20		25	ns
A, B, C, D		6.0				17		21	
		2.0				100		125	
Minimum Set-up time	t_{su}	4.5			11	20		25	ns
CLR		6.0		İ		17		21	
		2.0			_	0		0	
Minimum Hold time	t_h	4.5			_	0		0	ns
		6.0			_	0		0	
		2.0				150		190	
Minimum CLR	tw	4.5			16	30		38	ns
pulse width		6.0				26		33	
		2.0				100		125	
Minimum recovery time	t _{rem}	4.5			12	20		25	ns
		6.0				17		21	
		2.0		6			5		
Maximum clock	f max	4.5		30	56		24		MHz
frequency	- max	6.0		35	00		28		

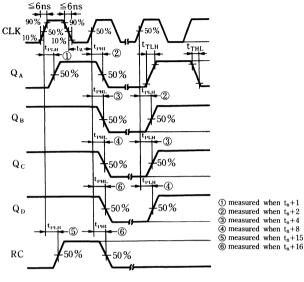
· Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit

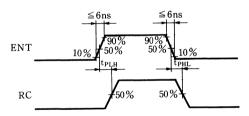


2. Waveforms

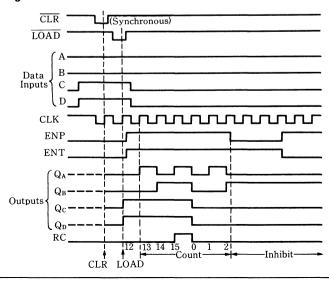
Waveforms-1 t PLH, t PHL (CLK \rightarrow Q A \sim Q D, RC)



Waveforms-2 t_{PLH} , t_{PHL} (ENL \rightarrow RC)



■ Typical Operating Conditions



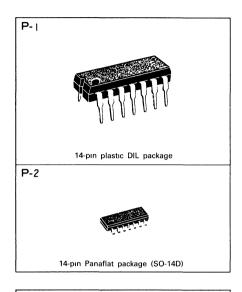
MN74HC164/MN74HC164S

8-Bit Serial-Input Parallel-Output Shift Register

■ Description

MN74HC164/MN74HC164S is 8-bit shift registor with gated serial input and asynchronous clear input. Gated serial input (A, B) control data input. When a LOW is applied to either or both, data input stops and the initial flip-flop is reset to "L" by the next clock pulse. When one input is "H", other inputs become enabled, and data is input to the initial flip-flop by the next clock pulse. Serial input data is not input, when clock is "H" or "L". But, data satisfying the set-up conditions clock rise at all times. Clear functions, when clear input is "L" regardless of clock.

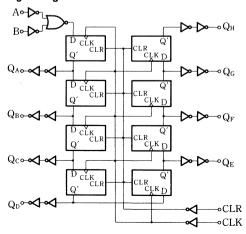
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

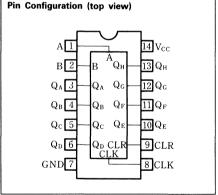


■ Truth table

	Input				Outpu	t	
CLR	CLK	A	В	Q _A	Q_B	•••	Q_H
L	×	×	×	L	L		L
Н	L	×	×	Q _{AO}	Q_{BO}		Q_{HO}
Н	5	Н	Н	Н	Q _{An}		Q Gn
Н	<i>_</i>	L	×	L	Q _{An}		Q _{Gn}
Н	5	×	L	L	Q _{An}		Q_{Gn}

■ Logic Diagram





■ Absolute Maximum Ratings

	Parameter	-	Symbol	Rating	Unit						
Supply voltag	Supply voltage			$-0.5 \sim +7.0$	V						
Ínput/output	output voltage		utput voltage		it voltage		tput voltage		$V_{\rm I}, V_{\rm O}$	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protect	tion diode current		I _{IK}	±20	mA						
Output paras	itic diode current		Іок	±20	mA						
Output curre	ent		Io	± 25	mA						
Supply curre	nt		I _{CC} , I _{GND}	±50	mA						
Storage temp	oerature range		Tstg	-65~+150	°C						
	MN74HC164	Ta=-40~+60℃	P_{D}	400	mW						
Power	MIN74HC104	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 8mW/°C	III VV						
dissipation	MN74HC164S	Ta=-40~+60℃	P_{D}	275	mW						
	MIN/4HC1045	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 3.8mW/°C	mvv						

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~V _{CC}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr,tf	4.5	0~500	ns
		6.0	0~400	ns

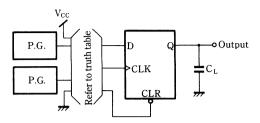
■ DC Characteristics (GND=0V)

			Те	st Conditi	ons		Г	`emperat	ure		
Parameter	Symbol	V _{CC}	17	Τ,		-	Γa=25°		Ta=-40	~ +85°C	Unit
		(V)	VI	Io	Unit	min.	typ.	max.	mın,	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_1 = V_{CO}$	or GNI	$I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

		Vcc			T	emperat	ure		
Parameter	Symbol	(V)	Test Conditions	-	Γa=25℃		Ta=-40	~+85°C	Unit
				min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15		19	ns
		6.0				13		16	
		2.0				150		190	
E Propagation time	tplh	4.5				30		38	ns
$CLK \rightarrow Q(L \rightarrow H)$		6.0				26		33	
		2.0				150		190	
E Propagation time	tPHL	4.5				30		38	ns
$CLK \rightarrow Q(H \rightarrow K)$		6.0				26	}	33	
		2.0	Physical Control of the Control of t			150		190	
E Propagation time	t _{PLH}	4.5				30		38	ns
$CLR \rightarrow Q(L \rightarrow H)$	1 2	6.0				26		33	
		2.0				150		190	
E Propagation time	tPHL	4.5				30		38	ns
$CLR \rightarrow Q(H \rightarrow L)$		6.0				26		33	
Name and the second sec		2.0				100		125	
Minimum pulse width	tw	4.5				20		25	ns
CLR		6.0				17		21	
Constant of the Constant of th		2.0				100		125	·
Minimum Set-up time	tsu	4.5				20		25	ns
		6.0				17		21	
		2.0				0		υ	
Hold time minimum	th	4.5			_	0		0	ns
		6.0			_	0		0	
The state of the s		2.0				75		95	
Minimum recovery time	trem	4.5				15		19	ns
		6.0				13		16	
		2.0		6			4		
Maximum clock	fmax	4.5		30			24		MH_Z
frequency		6.0		35			28		_

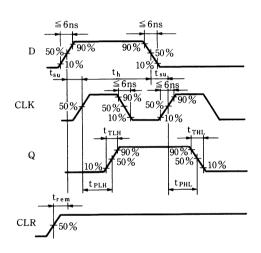
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Cırcuit

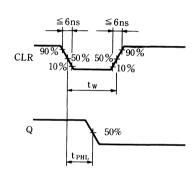


2. Waveforms

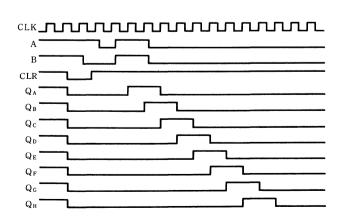
Waveforms-1
$$\begin{pmatrix} t_{\text{TLH}}, t_{\text{THL}}, t_{\text{PLH}}/t_{\text{PHL}}(CLK \rightarrow Q) \\ t_{\text{Su}}, \text{ fmax}, \text{ trem}, \text{ } t_h \end{pmatrix}$$

Waveforms-2 $(t_{PLH}/t_{PHL} (CLR \rightarrow Q), tw)$





■ Typical Operating Conditions



MN74HC165/MN74HC165S

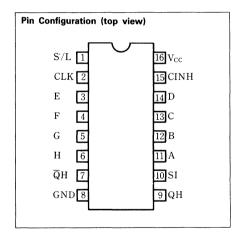
8-Bit Parallel-Input Serial-Output Shift Register

■ Description

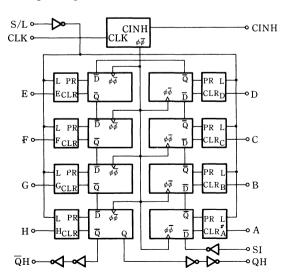
MN74HC165/MH74HC165S are high-speed 8-bit parallel-input/ serial output shift registor. The data is shifted from Q_A to Q_H by the clock. Parallel input at each stages works, when shift/load input is "L". These has gated clock input and complementary output from the 8th bit. When clock inhibit input is "L", the clock generates through 2 inputs NOR gate. When one of two clock inputs is "H", the internal clock stops. When shift/load input is "H", the other clock input works, if one of two clock input is maintained at LOW. The data is transferred by the rising edge of clock pulse. Parallel loading stops as long as shift/load input is "H". When shift/load input is "L", parrallel input data is directly loaded to the registor regardless of clock.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3 16-pin plastic DIL package P-4 16-pin Panaflat package (SO-16D)



■ Logic Diagram



■ Truth Table

		Input		l	ernal	Output	
				St	ages	·	
S/L	CINH	CLK	SI	A···H	Q_A	Qв	Qн
L	×	×	×	a…h	a	b	h
Н	L	L	×	×	\mathbf{Q}_{AO}	Q_{BO}	Q_{HO}
Н	L	<i></i>	Н	×	Н	Q_{An}	\mathbf{Q}_{Gn}
Н	L	5	L	×	L	Q_{An}	Q_{Gn}
Н	Н	×	×	×	Q _{AO}	Q_{BO}	Q _{HO}

■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit						
Supply voltag	Supply voltage		ply voltage		voltage		y voltage		Vcc	$-0.5 \sim +7.0$	V
Input/output	nput/output voltage			out/output voltage			$-0.5 \sim V_{CC} + 0.5$	V			
Input protect	tion diode current		I_{1K}	±20	mA						
Output paras	sitic diode current		Iok	±20	mA						
Output curre	ent		Io	± 25	mA						
Supply curre	nt		Icc, Icab	±50	mA						
Storage temp	perature range		Tstg	-65~+150	°C						
	MN74HC165	Ta=-40~+60℃	P_{D}	400	m W						
Power	WIN74HC103	$Ta = +60 \sim +85 ^{\circ}$	I I)	Decrease to 200mW at the rate of 8mW/°C	III VV						
dissipation	MN74HC165S	Ta=-40~+60℃	P_{D}	275	m W						
	WIN7411C1033	Ta=+60~+85℃	r ₁₎	Decrease to 200mW at the rate of 3.8mW/°C	m w						

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

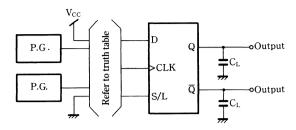
			Test Conditions								
Parameter	Symbol	(V)	Vı	I _o		,	Ta=25 °	C	Ta=-40	~+8 5 ℃	Unit
		(• /	VI		Unit	mın.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0]		4.2			4.2]	
		2.0						0.3		0.3	
Input LOW voltage	Vil	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	Vон	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	V _{II} .	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μΑ		0.0	0.1		0.1	V
-		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mΑ			0.32		0.37	
Input current	Ιι	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GNI	$I_0=0$			8.0		80.0	μA



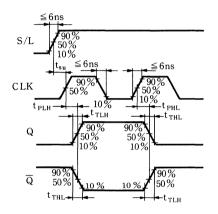
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

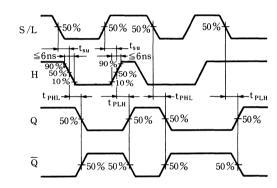
	1	Vcc			Te	mperat			
Parameter	Symbol	(V)	Test Conditions		Γa=25 °C	2	Ta=-40)~+85°C	Unit
				min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
P. P		2.0				150		190	
E Propagation time	t _{PLH}	4.5				30		38	ns
$CLK \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0		1		26		33	
7.5		2.0	With the second section of the second			150		190	
E Propagation time	t PHL	4.5				30	ł	38	ns
$CLK \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0				26		33	
P. P		2.0				150		190	
E Propagation time	t _{PLH}	4.5				30		38	ns
$S/L \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0				26		33	
		2.0				150		190	
E Propagation time	t _{PHL}	4.5				30		38	ns
$S/L \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0				26		33	
		2.0		 		150		190	
E Propagation time	t _{PLH}	4.5				30		38	ns
$H \rightarrow Q (L \rightarrow H)$	1 21 211	6.0				26	1	33	
		2.0				150		190	
E Propagation time	t PHL	4.5				30		38	ns
$H \rightarrow Q (H \rightarrow L)$	· rni.	6.0				26		33	
		2.0				150		190	
E Propagation time	t _{PLH}	4.5				30		38	ns
$H \rightarrow \overline{Q} (L \rightarrow H)$	C PI.H	6.0				26		33	
	 	2.0				150	 	190	
E Propagation time	t PHI.	4.5				30		38	ns
$H \rightarrow \overline{Q} (H \rightarrow L)$	rni.	6.0				26		33	5
	 	2.0				100		125	
Minimum Set-up time	t _{su}	4.5				20		25	ns
	-su	6.0				17		21	113
	<u> </u>	2.0			 	0	-	0	
Minimum Hold time	th	4.5			_	0		0	ns
Transition Hold thile	L P	6.0			_	0		0	113
	 	2.0		6	 	-	4	+ "	
Maximum clock	f _{max}	4.5		30		1	24		MHz
frequency	1 max	6.0		35			28		141112
	<u> </u>	0.0		30	L			\sqcup	

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

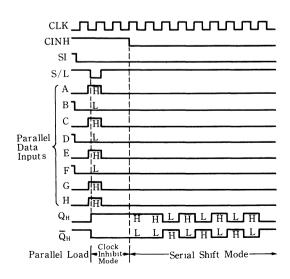


2. Waveforms





■ Typical Operating Conditions



MN74HC166/MN74HC166S

Parallel-load 8-bit shift Registers

■ Description

MN74HC166/MN74HC166S are high-speed, parallel-load 8-bit shift registers. The parallel-input or serial-input mode can be selected by the serial/load input.

When this input is HIGH, the serial-data input functions, and data are shifted from Q_A to Q_H by clock pulse.

When this input is LOW, however, the parallel-data input functions, and data are loaded by clock pulse.

When the input used as the clock pulse inhibit function is LOW, the internal clock pulses are generated through the two-input NOR gate.

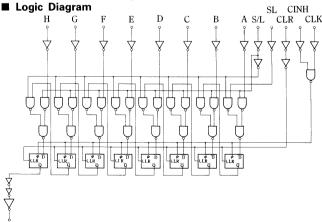
Internal clock pulses are inhibited when either one of the clock inputs is held at HIGH. Data transmission is made at the positive going edge of the clock pulse.

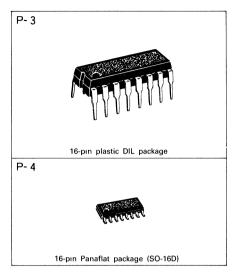
A buffer has been added to the gate output, thus improving the input/output transmission characteristics; fluctuations of the transmission time resulting from increasing the load capacity are suppressed to the minimum and, Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

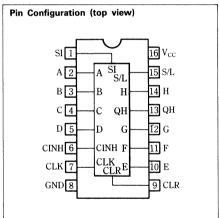
■ Truth Table

		I	nput					Output
CLR	S/L CINH CLK SI		SI	Parallel			Output	
CLK	3/L	CINII	CLK	31	AH	QA	QB	QH
L	×	×	×	×	×	L	L	L
Н	×	L	L	×	×	QA0	QB0	QH0
Н	L	L		×	a . h	а	b	h
Н	Н	L		Н	×	Н	QAn	QGn
Н	Н	L		L	×	L	QAn	QGn
Н	×	Н		×	×	QA0	QB0	QH0

Note: 1. ×: Either HIGH or Low; it doesn't matter







QΗ

■ Absolute Maximum Ratings

	Paramet	er	Symbol	Rating	Unit	
Supply voltage			V _{CC}	-0.5~+7.0	V	
Input/output	voltage		V _I , V _O	-0.5~V _{CC} +0.5	V	
Input protect	ion diode current		I _{IK}	±20	mA	
Output paras	itic diode current		l _{ok}	±20	mA	
Output curre	nt		Io	±25	mA	
Supply curre	nt		I _{CC} , I _{GND}	±50	mA	
Storage temp	perature range		Tstg	-65~+150	°C	
	MN74HC166	Ta=-40~+60°C	PD	400	***	
Power	WIN74IIC100	$Ta = +60 \sim +85^{\circ}C$] ''	Decrease to 200mW at the rate of 8mW/°C	mW	
dissipation	MN74HC166S	Ta=-40~+60°C	PD	275	mW	
	WIIV/411C1003	Ta=+60~+85°C	110	Decrease to 200mW at the rate of 3.8mW/°C	IIIW	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Ratıng	Unit
Operating supply voltage	V _{CC}		1.4~6.0	V
Input/output voltage	V _I		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		V _{CC} =2.0V	0~1000	ns
Input rise and fall time	t _r , t _f	V _{CC} =4.5V	0~500	ns
		$V_{CC}=6.0V$	0~400	ns

■ DC Characteristics (GND=0V)

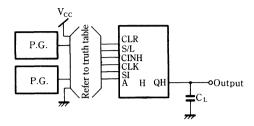
	:		Test Conditions				T	emperatu	re			
Parameter	Symbol	V _{CC} (V)	Vı	Io			Ta=25°C		Ta = -40	~+85°C	Unit	
		(,,	VI	10	Unit	mın.	typ.	max.	mın.	max.		
		2.0				1.5			1.5		V	
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V	
		6.0				4.2			4.2		V	
		2.0						0.3		0.3	V	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V	
		6.0						1.2		1.2	V	
		2.0		-20.0	μA	1.9	2.0		1.9		V	
		4.5	V_{IH}	-20.0	μ A	4.4	4.5		4.4		V	
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μ A	5.9	6.0		5.9		V	
		4.5	V_{IL}	-4.0	mA	3.86			3.76		V	
		6.0		-5.2	mA	5.36			5.26		V	
		2.0		20.0	μA		0.0	0.1		0.1	V	
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V	
Output LOW voltage	V _{OL}	6.0	or	20.0	μ A		0.0	0.1		0.1	V	
		4.5	V_{IL}	4.0	mA			0.32		0.37	V	
		6.0	:	5.2	mA			0.32		0.37	V	
Input current	I_{l}	6.0	$V_I = $	V _{CC} or G	ND			±0.1		+1.0	μA	
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CC}$	or GND	$I_{O}=0$			8.0		80.0	μΑ	



■ AC Characteristics (GND=0V, Input transistion tiem \leq 6ns, C_L =50pF)

					T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta = -40	~+85°C	Unit
		, ,		min.	typ.	max.	min.	max.	
		2.0			21	75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0	*		18	65		80	
Output fall time	t _{THL}	4.5			7	13		16	ns
_		6.0			6	11		14	
Propagation time		2.0			53	180		225	
CLK→QH	t _{PLH}	4.5			20	36		45	ns
(L→H)		6.0			17	31		38	
Propagation time		2.0			49	175		220	
CLK→QH	t _{PHL}	4.5			19	35		44	ns
(H→L)		6.0			16	30		37	
Propagation time		2.0			49	190		240	
CLR→QH	t _{PHL}	4.5			21	38		48	ns
(H→L)		6.0			18	32		41	
3.61	t _w	2.0			16	70		90	
Minimum pulse width CLR		4.5			8	14		18	ns
		6.0			7	12		15	
3.5		2.0			13	100		125	
Minimum Set-up time	t _{su}	4.5			3	20		25	ns
		6.0			2	17		21	
		2.0			_	0		0	
Minimum Hold time	t _h	4.5	,			0		0	ns
		6.0			_	0		0	
		2.0			5	75		95	
Minimum recovery time	T _{rem}	4.5			3	15		19	ns
		6.0			1	13		16	
		2.0		6	30		4		
Maximum clock frequency	f _{max}	4.5		30	70		24		MHz
		6.0		35	80		28		

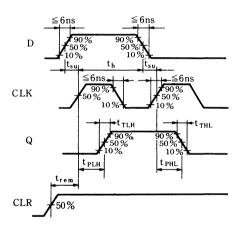
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

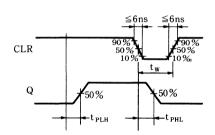


2. Waveforms

$$\begin{array}{c} \text{Waveforms-1} & \left(t_{\text{TLH, }} t_{\text{THL, }} t_{\text{su}}, f_{\text{max}}, \\ t_{\text{PLH/}} t_{\text{PHL}} (CLK \xrightarrow{} Q, \overline{Q}), t_{\text{rem, }} t_{h} \end{array} \right) \\ \end{array}$$

Waveforms-2 (tplh/tphl(CLR \rightarrow Q, \overline{Q}), tw)





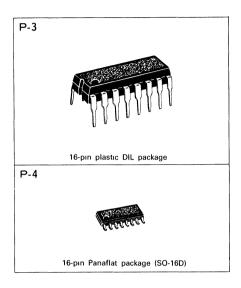
MN74HC173/MN74HC173S

Quad TRI-STATE D-Type Flip-Flops

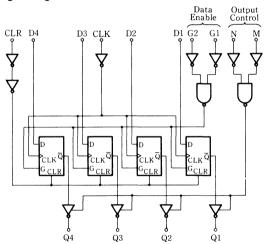
■ Description

MN74HC173/MN74HC173S are TRI-STATE quad D-type flip-flops. Quad D-type flip-flops is sysnchronously operated by common clock.

When one or either of output control (M, N) become "H", output turns to be tri-state mode and become ineffective. But, it doesn't effect the continuous operation of flip-flops. When one of data enable input (G1, G2) becomes "H", output Q is trasferred to input and remain flip-flops at the same condition. Clear operates, when clear input is "H". Date output operates on the rising edge of clock.Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

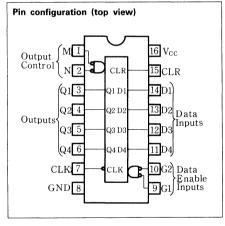


■ Logic Diagram



■ Truth Table

		Input			Output
CLR	CLV	Data	Enable	Data	
CLK	CLK	G1	G2	D	Q
Н	X	×	×	×	L
L	L	×	×	×	Qo
L	5	Н	×	×	Q_0
L	5	×	Н	×	Q_0
L	5	L	L	L	L
L	5	L	L	Н	Н



Note:

1. ×: Either HIGH or LOW; it doesn't matter

2. f: Rise of positive direction

3. Q_O: Q level prion to determination of input condition shown in table

 When one or either of M, N is "H", output turns to high impedence and becomes ineffective. But, it doesn't effect the continous operation of flip-flops.

■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit
Supply volta	Supply voltage			-0.5~+7.0	V
Input/output	voltage		V ₁ , V ₀	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	ction diode current		Iıĸ	±20	mA
Output para	sitic diode current		Іок	±20	mA
Output curre	Output current			±35	mA
Supply curre	ent		Icc, I GND	±70	mA
Storage tem	perature range		Tstg	-65~+150	°C
	MN74HC173	Ta=-40~+60℃	Pp	400	m W
Power	WINTAHCI75	Ta=+60~+85℃	L D	Decrease to 200mW at the rate of 8mW/°C	III VV
dissipation			D	275	117
	WIW 411C1733	Ta=+60~+85℃	P _D	Decrease to 200mW at the rate of 3.8mW/°C	m W

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

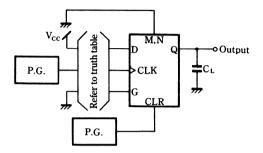
		V	Tes	t Conditio	ns		Te	emperat	ure		
Parameter	Symbol	V _{CC} (V)	V _I	Io			Ta=25℃	2	Ta=-40)~+85℃	Unit
			1 10	Unit	min.	typ.	max.	min.	max.		
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15		}	3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	Vон	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V _{1L}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36		Ì	5.26	İ	
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	Т	6.0	$V_I = V$	IH or V	IL			٠, ٥		+50	
current	Ioz	0.0	V _o =V	Vo=Vcc or GND				± 0.5		±5.0	μΑ
Quiescent supply current	$I_{\rm CC}$	6.0	$V_1 = V_0$	c or GNI	$I_0=0$			4.0		40.0	μA



■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

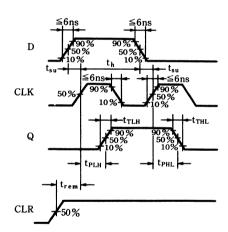
		V.	· · · · · · · · · · · · · · · · · · ·		Te	mperat	ure		
Parameter	Symbol	V _{CC}	Test Conditions		Ta=25℃		Ta=-40	~+85℃	Unit
		(1)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5		İ	7	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
Propagation time	toru	2.0				75		95	
CLK→Q (L→H)		4.5				15		19	ns
ΣLΛ(Q (L(Π)		6.0				13		16	
Propagation time		2.0				75		95	
CLK→Q (H→L)	t _{PHL}	4.5				15		19	ns
CLN-Q (N-L)		6.0				13		16	
Propagation time		2.0				150		190	
CLR→Q (H→L)	t _{PHL}	4.5				30		38	ns
CLR+Q (n+L)		6.0				26		33	
Minimum nuloo width		2.0				100		125	
CLR	finimum pulse width	4.5				20		25	ns
CLK		6.0				17		21	
2 -1 -1		2.0				100		125	
3-state propagation time	t _{PHZ}	4.5	$RL=1k\Omega$			20		25	ns
(H→Z)		6.0				17		21	
2 atata propagation time		2.0				125		155	
3-state propagation time	t _{PLZ}	4.5	$RL=1k\Omega$			25		31	ns
(L→Z)		6.0				21		26	
2 state propagation time		2.0				100		125	*****************
3-state propagation time	t _{PZH}	4.5	$R_L=1_k\Omega$			20		25	ns
(Z→ H)		6.0				17		21	
3-state propagation time		2.0				125		155	
	t _{PZL}	4.5	$R_L=1_k\Omega$			25		31	ns
(Z→L)		6.0				21		26	
		2.0				100		125	
Minimum Set-up time	tsu	4.5				20		25	ns
		6.0				17		21	
		2.0				0		0	
Minimum Hold time	th	4.5			_	0		0	ns
		6.0			-	0		0	
		2.0				100		125	
Minimum recovery time	t _{rem}	4.5				20		25	ns
-		6.0				17		21	
		2.0		6	†	<u> </u>	4		
Maximum clock frequency	f _{max}	4.5		30			24		MHz
		6.0		35	1		28		

- · Switching Time Measuring Circuit and Waveforms
- (1) ttlh, tthl, t_{su} , f_{max} , $t_{PLH}/t_{PHL}(CLK \rightarrow Q)$ $t_{PHL}(CLR \rightarrow Q)$, t_{w} , t_{rem} , t_{h}
 - 1. Measuring Circuit

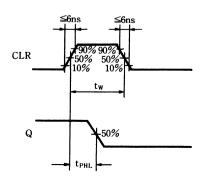


2. Switching Waveforms

Waveforms-1

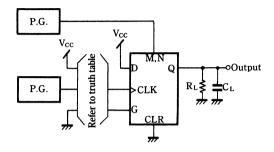


Waveforms-2

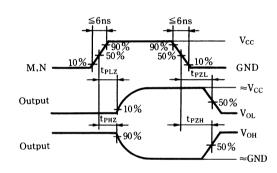


(2) tphz, tpzh

1. Measuring Circuit

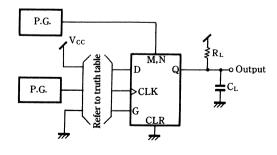


2. Switching Waveforms



(3) tplz, tpzl

1. Measuring Circuit



2. Switching Waveforms

See above [2] 2. for waveforms.



MN74HC174/MN74HC174S

Hex D-Type Flip-Flops with Clear

Description

MN74HC174/MN74HC174S contain six D-type flip-flop circuits with clear in one chip, and this master/slave flip-flop has common clock and clear. D-input data to be met to set-up time is transferred to output Q at the positive going edge of the clock pulse. When the clear input is "L", all outputs are set to "L". Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; LS TTL 10-inputs can be directly driven. Resistors and diodes are used in the $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

P-3 16-pin plastic DIL package P-4 16-pin Panaflat package (SO-16D)

■ Truth Table

	Input							
CLR	CLK	D	Q					
L	×	×	L					
Н	5	Н	Н					
Н	1	L	L					
Н	L	×	Q_0					

Note:

1. ____: Data input is transferred to output on the positive going edge from LOW to HIGH of the clock

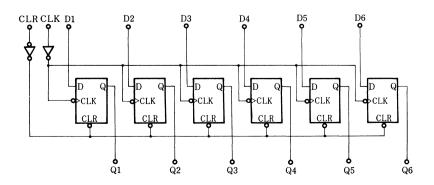
2. ×: Either HIGH or LOW; it doesn't matter

3. Q_O: Q level prior to determination of input condition shown in

table

Pin configuration (top view) CLR 1 16 V... Q1 2 15 Q6 D1 3 15 Q6 D2 4 1 1 10 Q4 Q2 5 1 10 Q4 GND 8 9 CLK

■ Logic Diagram



	Paramete	r	Symbol	Rating	Unit					
Supply voltage			Vcc	$-0.5 \sim +7.0$	V					
Input/output	Input/output voltage			output voltage		put voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	tion diode current		I _{IK}	±20	mA					
Output paras	sitic diode current		Іок	±20	mA					
Output curre	Output current			±25	mA					
Supply curre	ent		Icc, IGND	±50	mA					
Storage tem	perature range		Tstg	-65~+150	°C					
	MNIZALICIZA	Ta=-40~+60°C	D	400	m W					
Power	MN74HC174	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 8mW/°C	III VV					
dissipation	MN74HC174S	Ta=-40~+60℃	D	275	m W					
	WIN/4HC1/45	Ta=+60~+85℃	Pυ	Decrease to 200mW at the rate of 3.8mW/°C	m vv					

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V _I , V _O		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

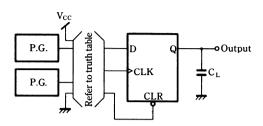
			Test Conditions			Tei	nperatu	re			
Parameter	Symbol	(V)	Vi	Io	т .		Ta=25 ℃			~+85℃	Unit
		(•)		10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	VII.	4.5						0.9		0.9	V
		6.0						1.2		1.2	
	Vон	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	Vih	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_i = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	Icc	6.0	$V_I = V_C$	cc or GNI	D, I ₀ =0			8.0		80.0	μA

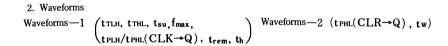


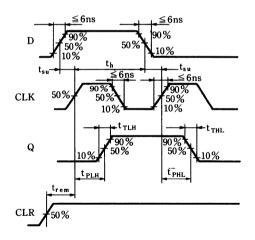
 \blacksquare AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

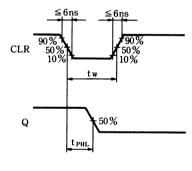
		37			T	emperat	ture		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Ta=25℃		Ta=-40	~+85℃	Unit
		``'		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
D		2.0				125		155	
Propagation time	t PLH	4.5			14	25		31	ns
$CLK \rightarrow Q (L \rightarrow H)$		6.0				21		26	
		2.0				125		155	
Propagation time	t PHL	4.5			14	25		31	ns
CLK→Q (H→L)		6.0		1		21		26	
D .: .:		2.0	· · · · · · · · · · · · · · · · · · ·		1	125		155	
Propagation time	t _{PHL}	4.5			17	25		31	ns
$CLR \rightarrow Q (H \rightarrow L)$		6.0				21	į	26	
		2.0				100		125	
Minimum Set-up time	t su	4.5			2	20		25	ns
		6.0				17		21	
		2.0				0		0	
Minimum Hold time	th	4.5				0		0	ns
		6.0				0		0	
		2.0				100		125	
Minimum pulse width	tw	4.5			8	20		25	ns
CLR		6.0				17		21	
		2.0				75		95	
Minimum recovery time	trem	4.5			1	15		19	ns
		6.0				13		16	
		2.0		6	20		4		
Maximum clock frequency	f _{max}	4.5		30	68		24		MHz
		6.0		35	70		28		

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})









MN74HC175/MN74HC175S

Quad D-Type Flip-Flops with Clear

■ Description

MN74HC175/MN74HC175S contain four quad D-type flip-flop circuits with clear, and this circuit has common clock and clear, and complementary outputs Q and \overline{Q} . D-input data is transferred to outputs Q and \overline{Q} at the rising edge of the clock pulse. The output from each flip-flop circuit is a reversed phase output of the other. All flip-flops are controlled by a common clock and clear; the clear function operates when the clear input is "L", and all Q and \overline{Q} outputs become "L" and "H" respectively. Adoption of the silicon gate CMOS process makes possible low power consumption and a high noise allowance; LS TTL 10-inputs can be directly driven. Resistors and diodes are used in the V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

■ Truth Table

	Input	Output			
CLR	CLK	D	Q	\overline{Q}	
L	×	×	L	Н	
Н	5	Н	Н	L	
Н	5	L	L	Н	
Н	L	×	Q_0	\overline{Q}_{o}	

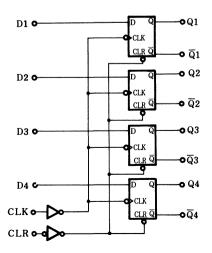
Note:

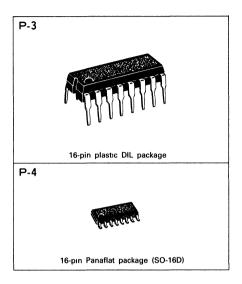
1. x: Data input is transferred to output on the negative-going edge from HIGH to LOW of the clock

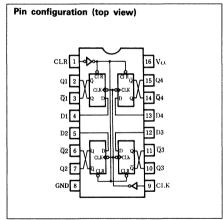
2. x: Either HIGH or LOW; it doesn't matter

3. Q_O: $(\overline{Q_O})$: $Q(\overline{Q})$ level prior to determination of input condition shown in table

■ Logic Diagram







Parameter			Symbol	Rating	Unit																						
Supply voltage	ge		voltage		$V_{\rm CC}$	-0.5~+7.0	V																				
Input/output	t/output voltage		it voltage		output voltage		put voltage		voltage		utput voltage		voltage		voltage		tput voltage		tput voltage		ıt voltage		out voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protect	tion diode current		I _{IK}	±20	mA																						
Output paras	sitic diode current		Іок	±20	mA																						
Output curre	Output current			±25	mA																						
Supply curre	nt		Icc, IGND	±50	mA																						
Storage temp	perature range		Tstg	-65~+150	C																						
	MN74HC175	Ta=-40~+60°C	P_{D}	400	117																						
Power	MIN74HC175	Ta=+60~+85℃	l rb	Decrease to 200mW at the rate of 8mW/°C	mW																						
dissipation	MN74HC175S	Ta=-40~+60°C	D	275	m W																						
	WW7411C1755	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m vv																						

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

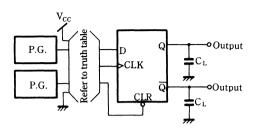
		,V _{CC} (V)	Test Conditions			T	emperat	ure			
Parameter	Symbol		Vı	Io r	Γ		Ta=25℃		Ta=-40	~+85℃	Unit
			V I	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{II} .	4.5						0.9		0.9	V
		6.0						1.2		1.2	
	Vон	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μ A		0.0	0.1		0.1	V
-		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_1	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GNI	$I_0 = 0$			8.0		80.0	μA



■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

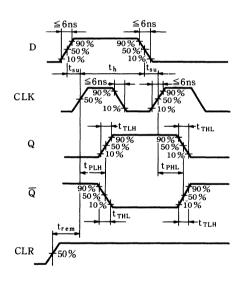
					Te	mperati	ıre		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Ta=25℃		Ta=-40)~ +85 ℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	t _{TLH}	4.5		}	8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t THL	4.5			7	15		19	ns
,		6.0			6	13		16	
\.		2.0				125		155	
Propagation time	t PLH	4.5			15	25		31	ns
$CLK \rightarrow Q, \overline{Q} (L \rightarrow H)$		6.0				21		26	
D		2.0				125		155	
Propagation time	t PHI.	4.5			15	25		31	ns
$CLK \rightarrow Q, \overline{Q} (H \rightarrow L)$		6.0				21		26	
D		2.0				175		220	
Propagation time	t _{PLH}	4.5			22	35	Ì	44	ns
$CLR \rightarrow \overline{Q} (L \rightarrow H)$		6.0				30		37	
D		2.0				150		190	
Propagation time	t PHI.	4.5			17	30		38	ns
$CLR \rightarrow Q (H \rightarrow L)$		6.0				26		33	
		2.0				100		125	
Minimum Set-up time	tsu	4.5			3	20		25	ns
		6.0				17		21	
		2.0				0		0	
Minimum Hold time	th	4.5			l	0		0	ns
		6.0			l —	0		0	
		2.0				100		125	
Minimum pulse width	t _w	4.5			8	20		25	ns
CLR		6.0				17	İ	21	
		2.0				75		95	
Minimum recovery time	t _{rem}	4.5			1	15		19	ns
		6.0				13		16	
		2.0		6			4		
Maximum clock frequency	fmax	4.5		30	66		24		MHz
		6.0		35			28		

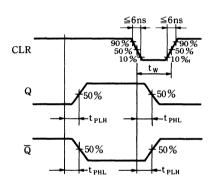
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit



2. Waveforms

Waveforms-2 $(t_{PLH}/t_{PHL}(CLR \rightarrow Q, \overline{Q}), t_{W})$





MN74HC183/MN74HC183S

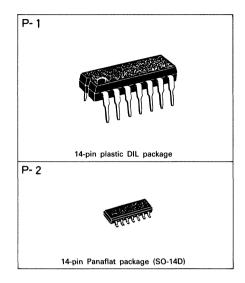
Dual Carry-Save Full Adders

■ Description

MN74HC183/MN74HC183S are dual carry-save full adders. Σ output is obtained by the sum of each bit, and the digit-carry signal from the 2nd bit's output is obtained in Cn+1 output.

Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

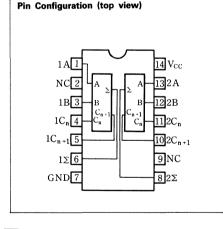


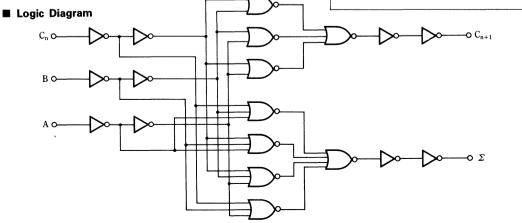
■ Truth Table

	Input	Output			
C_n	В	A	Σ	C_{n+1}	
L	L	L	L	L	
L	L	Н	Н	L	
L	Н	L	Н	L	
L	Н	Н	L	Н	
Н	L	L	Н	L	
Н	L	Н	L	Н	
Н	Н	L	L	Н	
Н	Н	Н	Н	Н	

Note:

1. H: High level 2. L: Low level





	Paramet	er	Symbol	Rating	Unit						
Supply voltage	age		oltage		voltage		voltage		V _{cc}	-0.5~+7.0	V
Input/output	put voltage		ıt voltage		V _I , V _O	-0.5~V _{CC} +0.5	v				
Input protect	ion diode current		I _{IK}	±20	mA						
Output paras	itic diode current		I _{OK}	±20	mA						
Output curre	nt		Io	±25	mA						
Supply curren	nt		I _{CC} , I _{GND}	±50	mA						
Storage temp	erature range		Tstg	-65~+150	°C						
	MN74HC183	Ta=-40~+60°C	PD	400	mW						
Power	WIN74IIC103	$Ta = +60 \sim +85^{\circ}C$] "	Decrease to 200mW at the rate of 8mW/°C	11174						
dissipation	MN74HC183S	Ta=-40~+60°C	PD	275	mW						
	MIN74HC1855	Ta=+60~+85°C	ΓD	Decrease to 200mW at the rate of 3.8mW/°C	11174						

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output	V _I , V _O		0~V _{CC}	V
Operating temperature range	T_{A}		-40~+85	°C
		V _{CC} =2.0V	0~1000	ns
Input rise and fall time	t ₄ , t _f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0V	0~400	ns

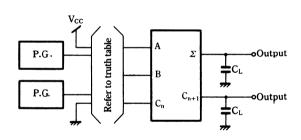
			Tes	t Condition	ons		Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	17	Ţ			Ta=25°C		Ta=-40	~+85°C	Unit
		(,,	V _I	$I_{\rm O}$	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	V
		2.0		-20.0	μΑ	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		v
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76	:	V
		6.0		-5.2	mA	5.36			5.26		V
		2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	V
Output LOW votlage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V _{IL}	4.0	mA			0.32		0.37	V
		6.0	l i	5.2	mA			0.32		0.37	V
Input current	Iı	6.0	V _I =	V _{CC} or G	ND			±0.1		±1.0	μΑ
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CC}$	or GND	, IO=0			8.0		80.0	μΑ

■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C_L=50pF)

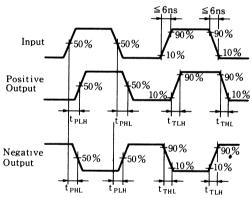
					Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta = -40	Unit	
		(,,		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5				15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5				15		19	ns
		6.0				13		16	
Propagation time		2.0				150		190	
A, B, $Cn \rightarrow \Sigma$, $Cn+1$	t _{PLH}	4.5				30		38	ns
(L→H)		6.0				26		33	
Propagation time		2.0				150		190	
A, B, $Cn \rightarrow \Sigma$, $Cn+1$	t _{PHL}	4.5				30		38	ns
(H→L)		6.0				26		33	

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms



MN74HC194/MN74HC194S

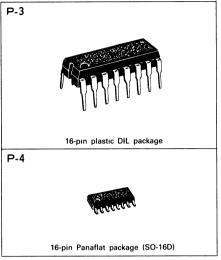
4-Bit Bidirectional Universal Shift Register

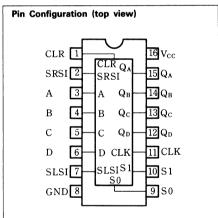
■ Description

MN74HC194/MH74HC194S is bidirectional shift register composed of parallel input, parallel output, right shift/left shift serial input, operating mode control, and direct clear input.

This register has four operating mode: parallel load, right shift (from Q_A to Q_D), left shift (from Q_D to Q_A), and clock stop. Synchronized parallel load is executed by applying four-bit data to the parallel input, when both mode control inputs S0 and S1 is "H". Data is loaded to the respective flip-flops, and transferred to the output on the rising edge of the clock. The serial shift stops during parallel loading. Right shift synchronizes with the clock pulse rise, when mode control input S0 is "H" and S1 is "L". When S0 is "L" and S1 is "H", left shift is executed by applying new data to the left shift serial input. The flip-flop clock stops when both mode control inputs are "L". Mode control input changes only when clock input is "H".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.





■ Truth Table

	_			Ing	out					Output			
CLR	Мо	ode	CLK	SLSI	SRSI		Para	allel		QA	Qв	$Q_{\rm C}$	0-
CLK	S1	S0	CLK	SLSI	SKSI	A	В	С	D	Q A	ØВ	₩c	Q_D
L	×	×	×	×	×	×	×	×	×	L	L	L	L
Н	×	×	L	×	×	×	×	×	×	Q _{Ao}	Q _{Bo}	Qc₀	Q_{Do}
Н	Н	Н	5	×	×	а	b	c	d	a	b	c	d
Н	L	Н	5	×	Н	×	×	×	×	Н	Q _{An}	Q _{Bn}	Q _{Cn}
Н	L	Н	5	×	L	×	×	×	×	L	Q _{An}	Q _{Bn}	Q _{Cn}
Н	Н	L	5	Н	×	×	×	×	×	Q _{Bn}	Q _{Cn}	Q_{Dn}	Н
Н	Н	L	5	L	×	×	×	×	×	Q _{Bn}	Q _{Cn}	Q_{Dn}	L
Н	L	L	×	×	×	×	×	×	×	Q _{Ao}	Q _{Bo}	Qc _o	Q_{Do}

Note: 1. H: HIGH 2. L: LOW 3. X: Either H or L, it doesn't matter

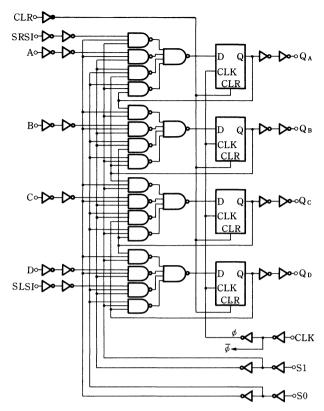
4. f: Rise from "L" to "H" 5. a, b, c, d: Input level of A, B, C, D on the normal condition

6. Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} : Q_A , Q_B , Q_C , Q_D level prion to the determination of input conditions shown in table.

7. Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}: Q_A, Q_B, Q_C, Q_D level before trasmition



■ Logic Diagram



■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit
Supply volta	age		$V_{\rm CC}$	$-0.5 \sim +7.0$	V
Input/output	tput voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	tion diode current		I_{1K}	±20	mA
Output paras	sitic diode current		Ioĸ	±20	mA
Output curre	ent		Io	±25	mA
Supply curre	ent	*	Icc, IGND	±50	mA
Storage tem	perature range		Tstg	−65~+150	${\mathbb C}$
	MN74HC194	Ta=-40~+60°C	P_{D}	400	mW
Power	MN74HC194	Ta=+60~+85 ℃	F)	Decrease to 200mW at the rate of 8mW/°C	m vv
dissipation	MN74HC194S	Ta=-40~+60℃	Po	275	m W
	1111141101945	Ta=+60~+85℃] P)	Decrease to 200mW at the rate of 3.8mW/°C	m w

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V ₁ ,V ₀		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Te	st Condition	ons		T	emperat	ure		
Parameter	Symbol	V _{CC} (V)	37	Io		,	Ta=25°	C	Ta=-40	~+85℃	Unit
		(v)	V _I	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5	-	
Input HIGH voltage	V _{iн}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{II} .	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	Vон	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μ A		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μ A		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Ιι	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	Icc	6.0	$V_I = V_C$	cc or GNI), I ₀ =0			8.0		80.0	μA

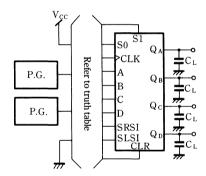
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

					To	mperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions	,	Ta=25 ℃		Ta=-40	~+85°C	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t TLH	4.5		:	8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				125		155	
CLK→Q (L→H)	t PLH	4.5				25		31	ns
CER FQ (E FII)		6.0				21		26	
Propagation time		2.0				125		155	
CLK→Q (H→L)	t PHI	4.5				25		31	ns
CER •Q (II •E)		6.0				21		26	
Propagation time		2.0				125		155	
	t PHI	4.5				25		31	ns
CLR→Q (H→L)		6.0				21		26	
Mınımum pulse width		2.0				100		125	
	t _w	4.5				20		25	ns
CLK, CLR		6.0				17		21	

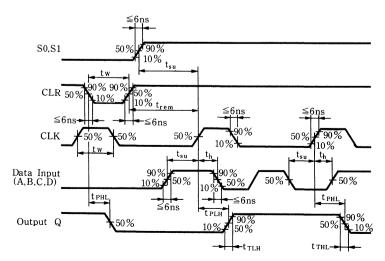
■ AC Characteristics (Cont'd)

				Te	mperat	ure			
Parameter	Symbol	Vcc	Test Conditions		Γa=25°C	;	Ta=-40	~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0				100		125	
Minimum Set-up time	tsu	4.5				20		25	ns
Time and the same	_	6.0				17		21	
		2.0				0		0	
Minimum Hold time	th	4.5			_	0		0	ns
		6.0			_	0		0	
		2.0				125		155	
Minimum recovery time	trem	4.5				25		31	ns
		6.0				21		26	
		2.0		6			4		
Maximum clock frequency	fmax	4.5		30			24		MHz
		6.0		35			28		

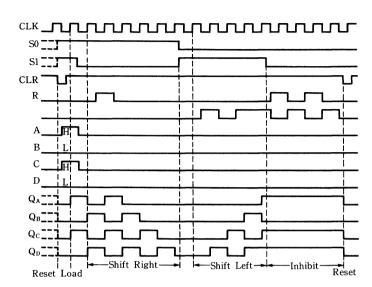
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit



2. Switching Waveforms



■ Typical Operating Conditions



MN74HC195/MN74HC195S

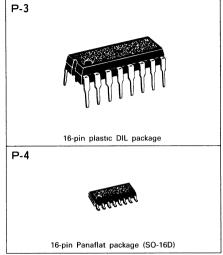
4-Bit Parallel Shift Register

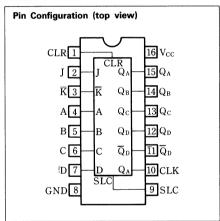
■ Description

MN74HC195/MH74HC195S are four-bit parallel shift registers composed of parallel input, parallel output, J- \overline{K} serial input, shift/load control input, and direct clear input. This shift register operates in two modes, parallel load and Q_A to Q_D . Parallel loading is executed y putting in four-bit data to a parallel input, and setting ."L" to the shift/load control input. Data is loaded to the respective flip-flop; output appears on the rising edge of clock pulse. The serial shift function stops between parallel loads. Serial shift is executed by the rising edge of clock pulse, when shift/load control input is "H" and data is input to the J- \overline{K} .

As shown in the truth table, the first stage represents to function as a $J-\overline{K}$, D, or toggle flip-flop.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.





■ Truth Table

				Input							Output		
CLR	SLC	CLK	Sei	ial		Para	allel		Q_A	Q_B	Qc	Q_{D}	$\overline{\overline{Q}}_{D}$
CLK	SLC	CLK	J	K	A	В	С	D	W/A	QΒ	W.C	A D	ďΒ
L	×	×	×	×	×	×	×	×	L	L	L	L	Н
Н	L	5	×	×	a	b	с	d	a	b	c	d	ā
Н	Н	L	×	×	×	×	×	×	Q _{Ao}	Q _{Bo}	Q _{Co}	Q_{Do}	$\overline{\overline{Q}}_{Do}$
Н	Н	5	L	Н	×	×	×	×	Q _{Ao}	Q _{Ao}	Q _{Bn}	Q_{Cn}	$\overline{\mathbf{Q}}_{Cn}$
Н	Н	5	L	L	×	×	×	×	L	Q _{An}	Q _{Bn}	Q _{Cn}	$\overline{\overline{\mathbf{Q}}}_{\mathbf{Cn}}$
Н	Н	5	Н	Н	×	×	×	×	Н	Q _{An}	Q _{Bn}	Q _{Cn}	$\overline{\overline{\mathbf{Q}}}_{\mathbf{Cn}}$
Н	Н	5	Н	L	×	×	×	×	Q An	Q _{An}	Q _{Bn}	Q _{Cn}	$\overline{\overline{\mathbf{Q}}}_{\mathbf{Cn}}$

Note:

1. H: HIGH 2. L:

LOW 3. ×:

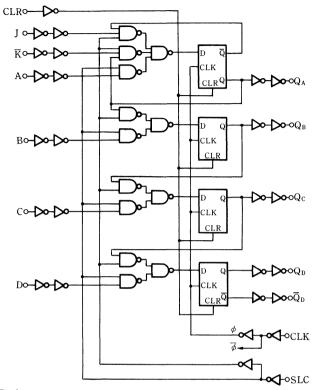
Either H or L, it doesn't matter

4. \mathcal{J} : Rise from "L" to "H" 5. a, b, c, d: Input level of A, B, C, D on the normal condition

6. Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}: Q_A, Q_B, Q_C, Q_D level prion to the determination of input conditions shown in table.

7. Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}: Q_A, Q_B, Q_C, Q_D level before trasmition

■ Logic Diagram



■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit
Supply voltag	ge		Vcc	$-0.5\sim+7.0$	V
Input/output	ut voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protect	tion diode current		I _{IK}	±20	mA
Output paras	itic diode current		Іок	±20	mA
Output curre	ent		Io	±25	mA
Supply curre	nt		Icc, IGND	±50	mA
Storage temp	perature range		Tstg	$-65 \sim +150$	${\mathbb C}$
	MNZALICIOE	Ta=-40~+60℃	D.	400	mW
Power	MN74HC195	Ta=+60~+85 ℃	P _D	Decrease to 200mW at the rate of 8mW/°C	III VV
dissipation	MN74HC195S	Ta=-40~+60℃	D	275	m W
	WIN/4HC1955	Ta=+60~+85 ℃	Po	Decrease to 200mW at the rate of 3.8mW/°C	m w

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_{I}, V_{O}		$0\sim V_{\rm CC}$	V
Operating temperature range	T_{A}		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

			Tes	st Condition	ons		Te	mperati	ıre		
Parameter	Symbol	V _{CC} (V)	V	Io		•	Ta=25°	2	Ta=-40	~+85℃	Unit
		(v)	Vı	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	VIL	4.5						0.9		0.9	v
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		200 200
		4.5	V _{IH}	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		2.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		4.5	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		6.0	0.1		0.1	V
		4.5	VIL	4.0	mA]	0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I ₁	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	cc or GNI), I ₀ =0			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

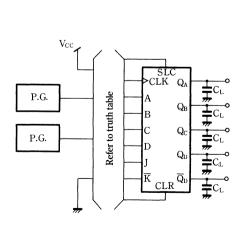
					Te	mperati	ıre		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Ta=25℃	2	Ta=-40)~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0			i	13		16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15	1	19	ns
		6.0				13	}	16	
		2.0				125		155	
E Propagation time	tPLH	4.5			}	25		31	ns
$CLK \rightarrow Q (L \rightarrow H)$		6.0				21		26	
E Propagation time		2.0				125		155	
CLK→Q (H→L)	t _{PHL}	4.5				25		31	ns
CLK-Q (H-L)		6.0				21	1	26	
P. D		2.0				150		190	
E Propagation time	t PLH	4.5				30		38	ns
$CLK \rightarrow \overline{Q} (L \rightarrow H)$		6.0				26		33	
E Propagation time		2.0				150		190	
	t PHL	4.5				30		38	ns
$CLK \rightarrow \overline{Q} (H \rightarrow L)$		6.0				26		33	
E. Duono antion tier -		2.0				125		155	
E Propagation time	t PHL	4.5				25		31	ns
CLR→Q (H→L)		6.0				21		26	

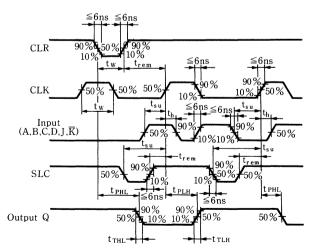
■ AC/Characteristics (Cont/d)

					Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Ta=25℃	2	Ta=-40)~+85℃	Unit
		,		min.	typ.	max.	min.	max.	
Management and a solidab		2.0				100		125	
Mınımum pulse width CLK, CLR	tw	4.5				20		25	ns
CLK, CLK		6.0				17		21	
		2.0				100		125	
Mınimum Set-up tıme	tsu	4.5				20		25	ns
		6.0				17		21	
		2.0			_	0		0	
Mınimum Hold time	th	4.5				0		0	ns
		6.0			_	0		0	
		2.0				75		95	
Minimum recovery time	trem	4.5				15		19	ns
		6.0				13		16	
		2.0		6			4		
Maximum clock frequency	fmax	4.5		30			24		MHz
nequency		6.0		35			28		

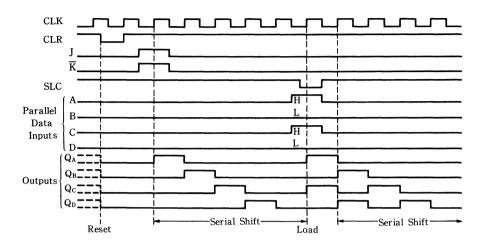
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

2. Waveforms





■ Typical Operating Conditions



MN74HC221/MN74HC221S

Dual Monostable Multivibrators with Clear

■ Description

MN74HC221/MN74HC221S are dual monostable multivibrator. Trigger input is triggered on falling edge of A input and rising edge of B input/CLR input. Once input is triggered, the monostable mode is sustained by a resitor and capacitor mounted externally, unless CLR input is "L".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Truth Table

]	[nput		Output			
CLEAR	A	В	Q	$\overline{\overline{\mathbf{Q}}}$		
L	×	×	L	Н		
×	Н	×	L	Н		
×	×	L	L	Н		
Н	L	5	J.	7_5		
Н	1	Н	Л	u		
5	L	Н	JZ	L		

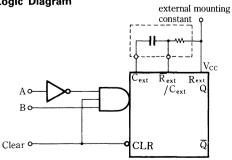
Note:

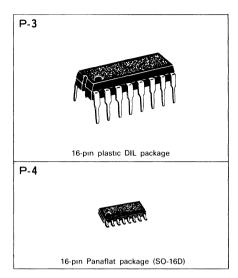
H: High level L: Low level

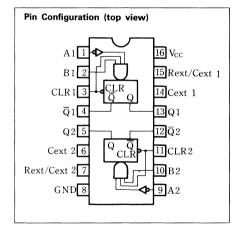
X: Either H or L, it doesn't matter

: fall from H to L
: use from L to H
: one High level pulse
: one Low level pulse

■ Logic Diagram









	Paramete	r	Symbol	Rating	Unit
Supply voltage	ge		Vcc	$-0.5 \sim +7.0$	V
Input/output	put/output voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protect	tion diode current		I_{IK}	±20	mA
Output paras	sitic diode current		Іок	±20	mA
Output curre	ent		Io	±25	mA
Supply curre	ent		Icc, Ignd	±50	mA
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$
	MN74HC221	Ta=-40~+60°C	P_{D}	400	m W
Power	MIN7411C221	Ta=+60~+85℃	F))	Decrease to 200mW at the rate of 8mW/°C	m vv
dissipation	MN74HC221S	Ta=-40~+60°C	р	275	m W
	WIN74HC2215	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m vv

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		2.0~6.0	V
Input/output voltage	V _I , V _O		0~Vcc	V
Operating temperature range	TA		$-40 \sim +85$	°C
Tourse and fall times		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
A, CLR		6.0	0~400	ns
external timing resistance	Rext		5~1000	kΩ
external timing capacitance	Cext		no limit	pF
wiring capacitance	Rext/Cext		0~50	pF

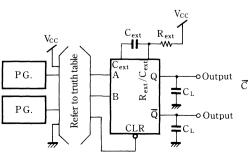
		**	Te	st Conditi	ons		T	emperat	ure		
Parameter	Symbol	V _{CC} (V)	Vı	Io		,	Ta=25℃	2	Ta=-40)~+85℃	Unit
			• 1	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{II} .	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	- 4.0	mA	3.86			3.76		
		6.0		- 5.2	mA	5.36			5.26		
		2.0		20.0	μΑ		0.0	0.1		0.1	
		4.5	V_{IH}	20.0	μ A		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
	,	6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
Rext/Cext pin	Lon	6.0	$V_I = V$	TH or V	11			+0 -		+5.0	
leak current	Ioz	0.0	$V_0 = V$	cc or G	ND			± 0.5		± 5.0	μΑ
Quiescent supply current	Icc	6.0	$V_I = V_C$	c or GNI	$I_0=0$			8.0		80.0	μA

 \blacksquare AC Characteristics (GND=0V, Input transition time ${\leq}6ns,~C_L{=}50pF)$

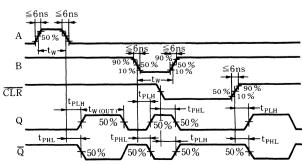
		.,			Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25 °	2	Ta=-40	0~+80℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			27	75		95	
Output rise time	t _{TLH}	4.5			10	15		19	ns
		6.0			8	13	1	16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			8	15		19	ns
		6.0			6	13	ł	16	
D		2.0			76	250		315	
Propagation time	t_{PLH}	4.5			28	50		63	ns
$A,B,CLR \rightarrow Q,(L \rightarrow H)$		6.0			20	43		54	
D		2.0			83	250		315	
Propagation time	t _{PHL}	4.5			29	50	}	63	ns
$A,B,CLR \rightarrow \overline{Q},(H \rightarrow L)$		6.0			22	43		54	
ъ.		2.0			47	150		190	
Propagation time	t _{PLH}	4.5			16	30		38	ns
$CLR \rightarrow Q, \ \overline{Q} \ (L \rightarrow H)$		6.0			15	26		33	
D		2.0			44	150		190	
Propagation time	t _{PHL}	4.5			16	30	1	38	ns
$CLR \rightarrow Q, \ \overline{Q} \ (H \rightarrow L)$		6.0			15	26		33	
		2.0	C + 0						
Propagation time	tw(out)	4.5	Cext = 0		78				ns
		6.0	$Rext = 5 k\Omega$		-				
		2.0	G . 1000 F		_				
Propagation time	tw(OUT)	4.5	Cext = 1000 pF		4.8		}		$\mu_{ extsf{S}}$
		6.0	$Rext = 10 k\Omega$		-				
		2.0				100		125	
Minimum pulse width	tw(IN)	4.5			9	20		25	ns
A, B		6.0				34		21	
3.6° 1 101		2.0				200		250	
Minimum pulse width	tw(IN)	4.5			21	40		50	ns
CLR		6.0		}	}	34	}	43	

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms





MN74HC237/MN74HC237S

3-to-8 Line Decoder with Address Latches

■ Description

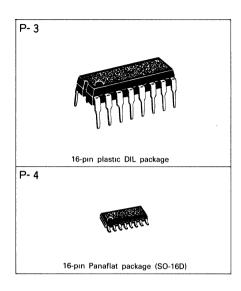
MN74HC237/MN74HC237S are high-speed 3-to-8 line decoders with three address latches. Address are stored, when \overline{GL} input is "H". When enable input G1 is "H" and G2 is "L", the output depending on A, B and C inputs become "H", and all other outputs become "L". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

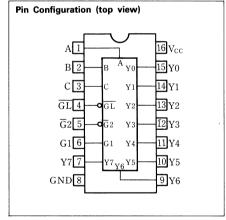
■ Truth Table

		Inp	ut						0				
I	Enable	е	,	Selec	t				Ou	put			
GL	G1	G2	С	В	A	Y0	Y1	Y2	Y 3	Y4	Y5	Y6	Y7
×	×	Н	×	×	×	L	L	L	L	L	L	L	L
×	L	×	×	×	×	L	L	L	L	L	L	L	L
L	Н	L	L	L	L	Н	L	L	L	L	L	L	L
L	H	L	L	L	Н	L	Н	L	L	L	L	L	L
L	H	L	L	Н	L	L	L	Н	L	L	L	L	L
L	Н	L	L	Н	Н	L	L	L	Н	L	L	L	L
L	Н	L	Н	L	L	L	L	L	L	Н	L	L	L
L	Н	L	Н	L	Н	L	L	L	L	L	Η	L	L
L	H	L	Н	Н	L	L	L	L	L	L	L	Н	L
L	Н	L	Н	Н	Н	L	L	L	L	L	L	L	Н
Н	Н	L	×	×	×				spond I othe			ed	

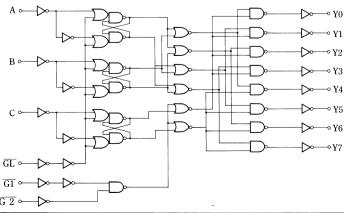
Note:

- 1. H: HIGH level
- 2. L: LOW level
- 3. ×: Either HIGH or LOW; doesn't matter





■ Logic Diagram



	Paramet	er ,	Symbol	Rating	Unit
Supply voltage	ge		V _{CC}	-0.5~+7.0	V
Input/output	voltage		V _I , V _O	-0.5~V _{CC} +0.5	V
Input protect	ion diode current		I_{IK}	±20	mA
Output paras	itic dıode current		I _{OK}	±20	mA
Output curre	nt		Io	±25	mA
Supply curre	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	oerature range		Tstg	-65~+150	°C
	MN74HC237	Ta=-40~+60°C	PD	400	mW
Power	WIN7411C237	$Ta = +60 \sim +85^{\circ}C$		Decrease to 200mW at the rate of 8mW/°C	11174
dissipation	MN74HC237S	$Ta = -40 \sim +60^{\circ}C$	PD	275	mW
	WIN7411C2373	$Ta = +60 \sim +85^{\circ}C$	10	Decrease to 200mW at the rate of 3.8mW/°C	11144

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	$V_{\rm I}, V_{\rm O}$		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		V _{CC} =2.0V	0~1000	ns
Input rise and fall time	t_r , t_f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0V	0~400	ns

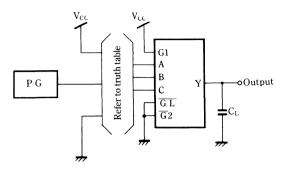
			Tes	t Conditio	ons		T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vı	ī			Ta=25°C		Ta=-40	~+85°C	Unit
		(,,	V _I	$I_{\rm O}$	Unit	mın.	typ.	max.	min.	max.	
		2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	V
		2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{1H}	-20.0	μΑ	4.4	4.5		4.4		V
Ouptut HIGH voltage	V_{OH}	6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	V _{IL}	-4.0	mA	3.86			3.76		V
		6.0		-5.2	mA	5.36			5.26		V
		2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μΑ		0.0	0.1		0.1	V
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	II	6.0	V _I =	V _{CC} or G	ND			±0.1		±1.0	μA
Quiescent supply current	I _{CC}	6.0	$V_I = V_{CC}$	or GND	, $I_O=0$			8.0		80.0	μΑ



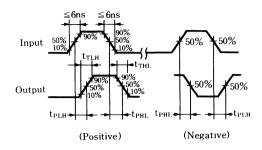
■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C₁=50pF)

		,,			Te	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta = -40	~+85°C	Unıt
		(,,		mın.	typ.	max.	min.	max.	
		2.0			22	75		95	
Output rise time	t _{TLH}	4.5			9	15		19	ns
		6.0			8	13		16	
		2.0			19	75		95	
Output fall time	t _{THL}	4.5			8	15		19	ns
		6.0			7	13		16	
Propagation time		2.0			48	150		190	
A, B, $\overline{C} \rightarrow Y$	t _{PLH}	4.5			22	30		38	ns
(L→H)		6.0			20	26		33	
Propagation time		2.0			40	150		190	
A, B, $C \rightarrow Y$	t_{PHL}	4.5			23	30		38	ns
$(H \rightarrow L)$		6.0			20	26		33	
Propagation time		2.0			47	150		190	
$GL \rightarrow Y$	t _{PLH}	4.5			22	30		38	ns
(L→H)		6.0			19	26	Ì	33	
Propagation time		2.0			50	150		190	
GL→Y	t _{PHL}	4.5			20	30		38	ns
$(H \rightarrow L)$	1	6.0			18	26		33	
Duono motion timo		2.0			34	150		190	
Propagation time $G1 \rightarrow Y$	PLH	4.5			17	30		38	ns
$(L \rightarrow H)$	1	6.0			15	26		33	
D		2.0		1	33	150		190	
Propagation time G1→Y	t _{PHL}	4.5			17	30		38	ns
$(H \rightarrow Y)$	1115	6.0			15	26		33	
D	_	2.0			33	125		155	
Propagation time $G2 \rightarrow Y$	t _{PLH}	4.5			17	25		31	ns
$(L \rightarrow H)$	1 21	6.0			16	21		26	
D .: .:		2.0		-	32	125		155	
Propagation time $\overline{G}2\rightarrow Y$	t _{PHL}	4.5			17	25		31	ns
(H→L)	- The	6.0			16	21		26	
		2.0			≦6	100		125	
Mınımum pulse width	t _w	4.5			<u>≤</u> 6	20		25	ns
GL	- w	6.0			<u>≤</u> 6	17		21	
3.6	-	2.0		+	17	100	-	125	
Minimum Set-up time	t _{su}	4.5			3	20		25	ns
A, B, C	-su	6.0			2	17		21	113
	+	2.0		+	<u> </u>	75		95	
Minimum Hold time	t.	4.5				15		19	ns
	t _h	6.0		1		13	1	16	115

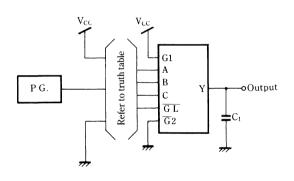
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit



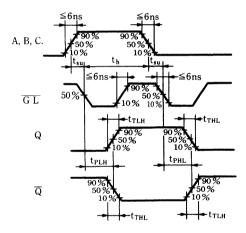
2. Waveforms



1. Measuring Circuit (t_{PLH},t_{PHL})



2. Waveforms





MN74HC238/MN74HC238S

3-to-8 Line Decoder/Demultiplexer

■ Description

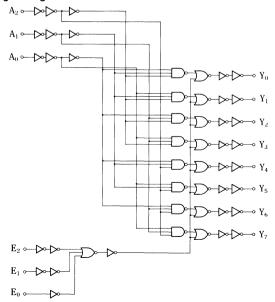
MN74HC238/MN74HC238S are high-speed 3-to-8 decoder/demultiplexer decoding one of eight output lines depending on the condition of three select inputs (A0, A1 and A2) and threes enable inputs ($\overline{E1}$, $\overline{E2}$ and E3). The enable input consists of an active LOW of 2 inputs and active HIGH of 1-input which makes the subsidiary connection easy. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

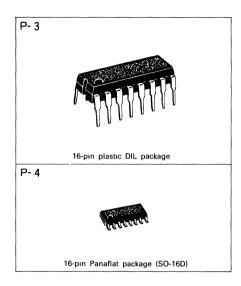
■ Truth Table

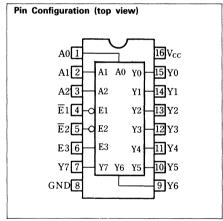
		Inp	out			Output							
E1	$\overline{\mathbf{E}}$ 2	E3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Н	×	×	×	×	×	L	L	L	L	L	L	L	L
×	Н	×	×	×	×	L	L	L	L	L	L	L	L
×	×	L	×	×	×	L	L	L	L	L	L	L	L
L	L	Н	L	L	L	Н	L	L	L	L	L	L	L
L	L	Н	L	L	Н	L	Н	L	L	L	L	L	L
L	L	Н	L	Н	L	L	L	Н	L	L	L	L	L
L	L	Н	L	Н	Н	L	L	L	Н	L	L	L	L
L	L	Н	Н	L	L	L	L	L	L	Н	L	L	L
L	L	Н	Н	L	Н	L	L	L	L	L	Н	L	L
L	L	Н	Н	Н	L	L	L	L	L	L	L	Н	L
L	L	Н	Н	Н	Н	L	L	L	L	L	L	L	Н

Note: 1. H: HIGH level 2. L: LOW level

■ Logic Diagram







	Paramet	er	Symbol	Rating	Unit		
Supply voltage	Supply voltage			−0.5~+7.0	V		
Input/output	Input/output voltage			-0.5~V _{CC} +0.5	v		
Input protect	Input protection diode current			±20	mA		
Output paras	itic diode current		I _{OK}	±20	mA		
Output curre	nt			I _O ±25			
Supply curre	nt		I _{CC} , I _{GND}	±50	mA		
Storage temp	erature range		Tstg	-65~+150	°C		
	MN74HC238	$Ta = -40 \sim +60^{\circ}C$	PD	400	mW		
Power	WIN7411C236	$Ta = +60 \sim +85^{\circ}C$		Decrease to 200mW at the rate of 8mW/°C	11144		
dissipation	MN74HC238S	Ta=-40~+60°C	PD	275	mW		
	WITT-411C2363	$Ta = +60 \sim +85^{\circ}C$		Decrease to 200mW at the rate of 3.8mW/°C	11177		

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output	V _I , V _O		0~V _{CC}	V
Operating temperature range	TA		−40~+85	°C
		V _{CC} =2.0V	0~1000	ns
Inupt rise and fall time	t _r , t _f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0V	0~400	ns

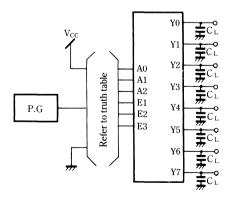
			Tes	t Conditio	ons		Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vı	ı			Ta=25°C		Ta=-40	~+85°C	Unit
		(,,	V _I	Io	Unit	min.	typ.	max.	mın.	max.	
		2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	V
		2.0		-20.0	μΑ	1.9	2.0		1.9		V
		4.5	V _{IH}	-20.0	μΑ	4.4	4.5		4.4		V
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	V_{IL}	-4.0	mA	3.86		ĺ	3.76		V
		6.0		-5.2	mA	5.36			5.26		V
		2.0		20.0	μΑ		0.0	0.1		0.1	V
		4.5	V _{IH}	20.0	μΑ		0.0	0.1		0.1	V
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I _I	6.0	$V_I =$	V _{CC} or G	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CC}$	or GND	$I_{O}=0$			8.0		80.0	μΑ

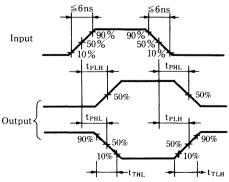
■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C_L=50pF)

					T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta=-40	~+85°C	Unit
		(,,		min.	typ.	max.	mın.	max.	
		2.0			21	75		95	
Output rise time	t_{TLH}	4.5			6	15		19	ns
		6.0			5	13		16	
		2.0			13	75		95	
Output fall time	t _{THL}	4.5			5	15		19	ns
		6.0			4	13		16	
Propagation time		2.0			36	150		190	_
$A \rightarrow Y$	t_{PLH}	4.5			13	30		38	ns
(L→H)		6.0			11	26		33	
Propagation time		2.0			33	150		190	
$A \rightarrow Y$	t_{PHL}	4.5			13	30		38	ns
(H→L)		6.0			11	26		33	
Propagation time		2.0			49	150		190	
$\overline{E}1, \overline{E}2 \rightarrow Y$	t _{PLH}	4.5			16	30		38	ns
$(L \rightarrow H)$		6.0			13	26		33	
Propagation time		2.0			41	150		190	
$\overline{E}1, \overline{E}2 \rightarrow Y$	t _{PHL}	4.5			16	30		38	ns
(H→L)		6.0			13	26		33	
Propagation time		2.0			41	150		190	
E3→Y	t _{PLH}	4.5			15	30		38	ns
$(L \rightarrow H)$		6.0			12	26		33	
Propagation time		2.0			40	150		190	
E3→Y	t _{PHL}	4.5			15	30		38	ns
$(H \rightarrow L)$		6.0			13	26		33	

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

2. Waveforms





MN74HCT238/MN74HCT238S

3-to-8 Decoder/Demultiplexer (TTL Input)

■ Description

MN74HCT238/MN74HCT238S are high-speed 3-to-8 decoder/demultiplexer (TTL input) decoding one of eight output lines depending on the condition of three select inputs (A0, A1 and A2) and threes enable inputs (E1, E2 and E3). The input consists of an active LOW of 2 inputs and active HIGH of 1-input which makes the subsidiary connection easy. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2V or more is logic "1". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

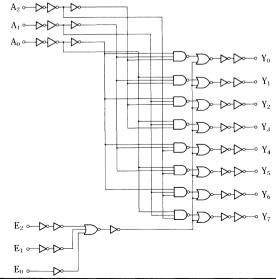
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

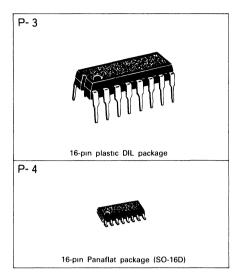
■ Truth Table

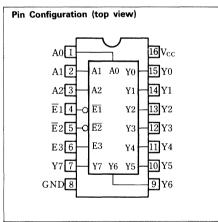
		Inp	out						Out	put			
E ₁	E2	ЕЗ	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Н	×	×	×	×	×	L	L	L	L	L	L	L	L
×	Н	×	×	×	×	L	L	L	L	L	L	L	L
×	×	L	×	×	×	L	L	L	L	L	L	L	L
L	L	Н	L	L	L	Н	L	L	L	L	L	L	L
L	L	Н	L	L	Н	L	Н	L	L	L	L	L	L
L	L	Н	L	Н	L	L	L	Н	L	L	L	L	L
L	L	Н	L	Н	Н	L	L	L	Н	L	L	L	L
L	L	Н	Н	L	L	L	L	L	L	Н	L	L	L
L	L	Н	Н	L	Н	L	L	L	L	L	Н	L	L
L	L	Н	Н	Н	L	L	L	L	L	L	L	Н	L
L	L	Н	Н	Н	Н	L	L	L	L	L	L	L	Н

Note: 1. H: HIGH level 2. L: LOW level

■ Logic Diagram







	Paramet	er	Symbol	Rating	Unit				
Supply voltage	Supply voltage			-0.5~+7.0	V				
Input/output	nput/output voltage			-0.5~V _{CC} +0.5	V				
Input protect	tion diode current	iode current		n diode current		n diode current		±20	mA
Output paras	itic diode current		I _{OK}	±20	mA				
Output curre	ent			I _O ±25					
Supply curre	nt		I _{CC} , I _{GND}	±50	mA				
Storage temp	perature range		Tstg	−65~+150	°C				
	MN74HC238	Ta=-40~+60°C	PD	400	mW				
Power	WIN74HC256	$Ta = +60 \sim +85^{\circ}C$	7 1	Decrease to 200mW at the rate of 8mW/°C	111 44				
dissipation	MN74HC238S	Ta=-40~+60°C	PD	275	mW				
	MIN74HC2365	$Ta = +60 \sim +85^{\circ}C$	FD	Decrease to 200mW at the rate of 3.8mW/°C	11144				

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{CC}		4.5~5.5	V
Input/output	V _I , V _O		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
Inupt rise and fall time	t _r , t _f	4.5V	0~500	ns

		**	Tes	t Condition	ons		Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vī	I_{O}			Ta=25°C		Ta = -40	~+85°C	Unit
		(,,	v I	10	Unit	min.	typ.	max.	min.	max.	
		4.5									
Input HIGH voltage	V_{IH}	≀				2.0			2.0		V
		5.5						ļ			
		4.5		•							
Input LOW voltage	V_{IL}	≀						0.8		0.8	V
		5.5									
		4.5	V _{IH}	-20.0	μΑ	4.4	4.5				
Output HIGH voltage	V_{OH}		or					}	4.4		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		V
		4.5	V _{IH}	20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	V_{OL}		or								V
		4.5	V_{IL}	4.0	mA			0.32		0.37	v
Input current	II	5.5	V _I =	V _{CC} or G	ND			±0.1		±1.0	μA
Quiescent supply current	I _{cc}	5.5	$V_I = V_{CC}$	or GND	, $I_O=0$			8.0		80.0	μΑ

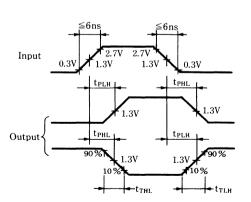
■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C_L=50pF)

					Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta=-40	~+85°C	Unit
				min.	typ.	max.	min.	max.	
Output rise time	t _{TLH}	4.5			5	15		19	ns
Output fall time	t _{THL}	4.5			4	15		19	ns
Propagation time $A \rightarrow Y$ $(L \rightarrow H)$	t _{PLH}	4.5			18	35		44	ns
Propagation time $A \rightarrow Y$ $(H \rightarrow L)$	t _{PHL}	4.5			13	30		38	ns
Propagation time \overline{E} 1, \overline{E} 2 \rightarrow Y $(L\rightarrow H)$	t _{PLH}	4.5			20	40		50	ns
Propagation time \overline{E} 1, \overline{E} 2 \rightarrow Y $(H\rightarrow L)$	t _{PHL}	4.5			16	30		38	ns
Propagation time $E3 \rightarrow Y$ $(L \rightarrow H)$	t _{PLH}	4.5			15	30		38	ns
Propagation time $E3 \rightarrow Y$ $(H \rightarrow L)$	t _{PHL}	4.5			21	40		50	ns

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

P.G.

2. Waveforms



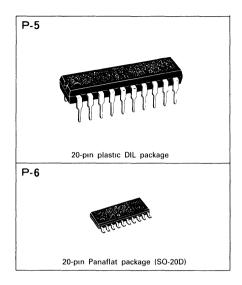


MN74HC240/MN74HC240S

Inverting Octal TRI-STATE Buffers

■ Description

MN74HC240/MN74HC240S are high-speed inverting buffers constructed with octal tri-state outputs. High-speed operation can be obtained for driving a large capacity bus line, because these ICs have large current output. When the output is "L", inputs $1\overline{G}$ and $2\overline{G}$ are available, where output becomes enable and each of the four buffers is independently controlled. Adoption of the silicon gate CMOS process makes possible low power consumption and a high noise allowance; LS TTL 15-inputs can be directly driven. Resistors and diodes are used in the V_{CC} and GND in order to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

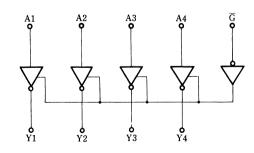


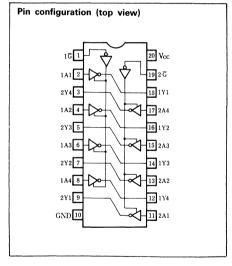
■ Truth Table

In	put	Output	Input		Output	
1 \overline{G}	1 A	1 Y	$2\overline{\mathrm{G}}$	2 A	2 Y	
L	L	Н	L	L	Н	
L	Н	L	I.	Н	L	
Н	L	Hı-Z	Н	L	Hi-Z	
Н	Н	Hı-Z	Н	Н	Hi-Z	

Note:

H₁-Z: High impedance





	Paramete	r	Symbol	Rating	Unit		
Supply voltag	oltage		roltage		Vcc	-0.5∼ +7.0	V
Input/output	Input/output voltage			$-0.5 \sim V_{CC} + 0.5$	V		
Input protec	Input protection diode current			± 20	mA		
Output paras	Output parasitic diode current			± 20	mA		
Output curre	Output current			± 35	mA		
Supply curre	ent		Icc, IGND	±70	mA		
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$		
	MNZALICOAO	$Ta = -40 \sim +60 ^{\circ}$	P_{D}	400	mW		
Power	Power MN74HC240 $Ta = +60 \sim +85^{\circ}$		r _D	Decrease to 200mW at the rate of 8mW/°C	m vv		
dissipation	dissipation MN74HC240S $Ta = -40 \sim +60 ^{\circ}$		D.	275	m W		
	MIN/4HC240S	Ta=+60~+85°C	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m vv		

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_{I}, V_{O}		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

		1,7	Te	st Condition	ons		Te	mperati	ıre		
Parameter	Symbol	(V)	Vı	Io			Γa=25°	2	Ta=-40)~+85℃	Unit
			V 1	1()	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	Vih	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{II} .	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	ViH	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	Vон	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VfL	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1	1	0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1	l	0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μ A	1	0.0	0.1	}	0.1	V
		4.5	VIL	6.0	mA			0.32	1	0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Ιı	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μΑ
3-state output off state	Ioz	6.0	$V_1 = V$	IH or V	II.			±0.5		±5.0	μΑ
current	10Z	0.0	$V_0 = V$	lcc or C	GND			⊥0.5		13.0	μΑ
Quiescent supply current	$I_{\rm CC}$	6.0	$V_1 = V_0$	c or GNI	$I_0 = 0$			8.0		80.0	μA



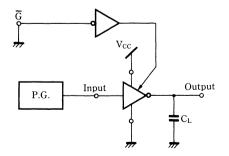
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

					Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions	,	Γa = 25°	2	Ta=-40)~+85°C	Unit
		(*)		min.	typ.	max.	min.	max.	
	-	2.0				75		95	
Output rise time	t TLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time t ₁	t THL	4.5			6	15	l	19	ns
		6.0				13		16	
Propagation time $(L \rightarrow H)$ t_{PLH}		2.0				75		95	
	4.5			8	15		19	ns	
		6.0				13		16	
		2.0				75		95	
Propagation time	t _{PHL}	4.5			8	15		19	ns
(H→L)		6.0				13		16	
0		2.0	and the second s			125		155	J
3-state propagation time	t PHZ	4.5	$R_L = 1 k\Omega$		14	25		31	ns
$(H \rightarrow Z)$		6.0				21		26	
0		2.0				150		190	
3-state propagation time	t PLZ	4.5	$R_L = 1 k\Omega$		17	30		38	ns
$(L \rightarrow Z)$		6.0				26		33	
		2.0				100		125	
3-state propagation time	t _{PZH}	4.5	$R_L = 1 k\Omega$		12	20	1	25	ns
(Z→H)		6.0				17		21	
		2.0				100		125	
3-state propagation time	t PZL	4.5	$R_L = 1 k\Omega$		13	20	1	25	ns
(Z→L)		6.0				17		21	

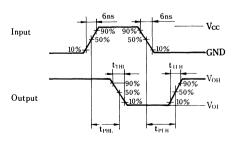
• Switching Time Measuring Circuit and Waveforms

[1] t_{TLH} , t_{THL} , t_{PLH}/t_{PHL}

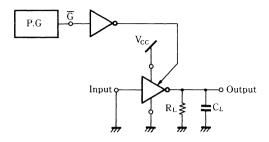
1. Measuring Circuit (t_{PLH},t_{PHL})

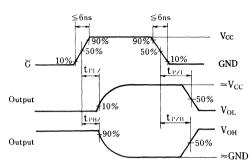


2. Waveforms

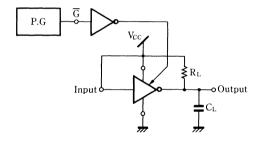


- (2) tphz, tpzh
 - 1. Measuring Circuit





- (3) tplz, tpzl
 - 1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

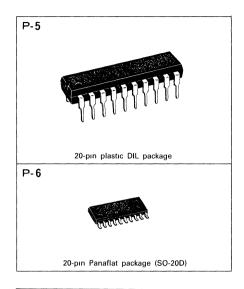


MN74HC241/MN74HC241S

Octal TRI-STATE Buffer

■ Description

MN74HC241/MN74HC241S are high-speed non-inverted buffers constructed with octal tri-state outputs. High-speed operation can be obtained for driving a large capacity bus line, because these ICs have large current outputs. Also, these ICs have input $1\overline{G}$ where output becomes enable at "L" output, and input 2G where output becomes enable at "H" output, and each of the four buffers is independently controlled. Adoption of the silicon gate CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; LS TTL 15-inputs can be directly drive. Resistors and diodes ar used in the V_{CC} and GND in order to protect the input/output from damage by static electricity. Same pin configuration and function as standard 45LS/74LS Logic Family.



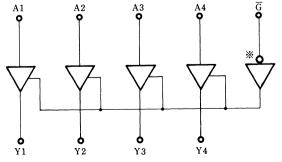
■ Truth Table

Ing	Input		In	Output	
1 G	1 A	1 Y	2G	2 A	2 Y
L	L	L	L	L	Hı-Z
L	Н	Н	L	Н	Hı-Z
Н	L	Hi-Z	Н	L	L
Н	Н	Hi-Z	Н	Н	Н

Note:

1. Hi-Z: High impedance

Pin configuration (top view) 20 Vcc 1A1 2 19 2G 274 3 18 171 1A2 4 177 2A4 273 5 16 172 1A3 6 15 2A3 272 7 14 173 1A4 8 13 2A2 271 9 12 174 GND 10 11 2A1





	Paramete	r	Symbol	Rating	Unit			
Supply voltag	roltage		ltage		Vcc	−0.5∼ +7.0	V	
Input/output voltage			V_1, V_0	$-0.5 \sim V_{(c} + 0.5$	V			
Input protect	Input protection diode current			±20	mA			
Output paras	sitic diode current		I_{OK}	±20	mA			
Output curre	Output current			urrent		Io	±35	mA
Supply curre	urrent		Icc, IGND	±70	mA			
Storage temp	temperature range		Tstg	$-65 \sim +150$	°C			
	MN74HC241	Ta=-40~+60℃	P_{D}	400	W'			
Power	T 100 1050		r ()	Decrease to 200mW at the rate of 8mW/°C	m W			
dissipation	dissipation MN74HC241S $Ta = -40 \sim +60 ^{\circ}$		D	275	W			
	MIN/41102415	Ta=+60~+85℃	$P_{\rm D}$	Decrease to 200mW at the rate of 3.8mW/°C	m W			

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vec		1.4~6.0	V
Input/output voltage	$V_{\rm I}, V_{\rm O}$		0~V.α	V
Operating temperature range	TA		-40~+85	
		2.0	0~1000	ns
Input rise and fall time	tr,tf	4.5	0~500	ns
		6.0	0~400	ns

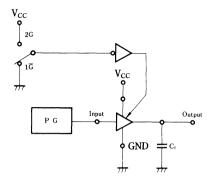
		$V_{\rm CC}$	Te	st Conditi	ons		Te	mperati	ıre	(Unit
Parameter	Symbol	(V)	Vı	Io		·	Γa=25℃	2	Ta=-40	0~+85℃	
				10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5		}		3.15			3.15]]	V
		6.0				4.2			4.2		
		2.0						0.3	İ	0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	V_{OH}	4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9	1 1	V
		4.5	V_{fL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μΑ		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1	1	0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_1	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state current	Ioz	6.0		IH or V				±0.5		±5.0	μΑ
Quiescent supply current	I_{CC}	6.0	$V_1 = V_0$	c or GNI	$I_0=0$			8.0		80.0	μA

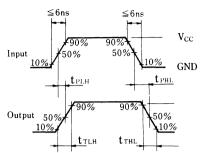


■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

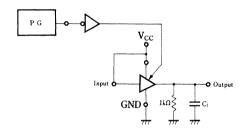
					Te	emperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25 °	2	Ta=-40)~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13		16	
Output fall time		2.0				75		95	
	t _{THL}	4.5	!		7	15		19	ns
		6.0				13		16	
Propagation time $(L \rightarrow H) \hspace{1cm} t_{PLH}$		2.0				75		95	
	t _{PLH}	4.5			8	15		19	ns
		6.0				13		16	
Propagation time		2.0				75		95	
(H→L)	t _{PHL}	4.5			7	15		19	ns
(n→L)		6.0				13		16	
3-state propagation time		2.0				125		155	
	t PHZ	4.5	$R_L = 1k\Omega$		14	25		31	ns
(H→Z)		6.0				21		26	
0 -1-1		2.0				100		125	
3-state propagation time	t _{PLZ}	4.5	$R_L=1k\Omega$		11	20		25	ns
(L→Z)		6.0				17		21	
2 atata ================================		2.0				100		125	
3-state propagation time	t _{PZH}	4.5	$R_L = 1k\Omega$		11	20		25	ns
(Z→H)		6.0				17		21	
2	- 10	2.0				100		125	
3-state propagation time	t PZL	4.5	$R_L=1k\Omega$		11	20		25	ns
(Z→L)		6.0				17		21	

- · Switching Time Measuring Circuit and Waveforms
- (1) ttlh, tthl, tplh, tphl
 - 1. Measuring Circuit

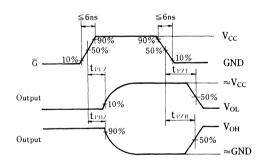




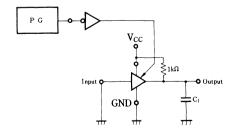
- (2) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit



2. Waveforms $(t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})$



- (3) t_{PLZ}, t_{PZL}
 - 1. Measuring Circuit





MN74HC242/MN74HC242S

Inverting Quad TRI-STATE Transceivers

■ Description

MN74HC242/MN74HC242S are high-speed tri-state output, inverting buffers which asynchronously transfer the input bidirectionally through the data bus line. Large current output makes possible high-speed operation for driving a large capacity bus line. These ICs have input GBA where output A becomes enable at "H" level, and input GAB where output B becomes enabled at "L" level. Adoption of the silicon gate CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; LS TTL 15-pints can be directly driven.

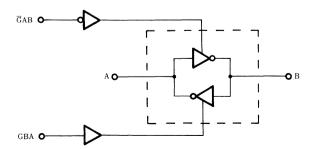
Resistors and diodes are used in the $V_{\rm CC}$ and GND in order to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

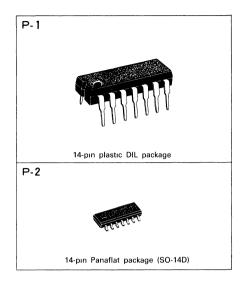
■ Truth Table

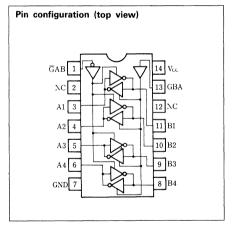
Contro	l Input	Data Port Status			
GAB	GBA	A	В		
Н	Н	OUTPUT	INPUT		
L	Н	*	*		
Н	L	Hı-Z	Hı-Z		
L	L	INPUT	OUTPUT		

Note:

- *: When the transceiver operates bi-directionally at the same time, destructive oscillation might occur.
- 2. Hi-Z: High impedance







	Parameter	r	Symbol	Rating	Unit				
Supply volta	oltage		voltage		oly voltage		Vcc	-0.5~+7.0	V
Input/output voltage			V_{I}, V_{O}	$-0.5 \sim V_{CC} + 0.5$	V				
Input protection diode current			Iik	± 20	mA				
Output parasitic diode current			Іок	± 20	mA				
Output curr	Output current			t current		Io	±35	mA	
Supply curre	ent		Icc, IGND	±70	mA				
Storage tem	temperature range		Tstg	-65~+150	$^{\circ}$				
	MN74HC242	$Ta = -40 \sim +60 ^{\circ}C$	P_{D}	400	W				
Power	MN74HC24Z	Ta=+60~+85°C	FD	Decrease to 200mW at the rate of 8mW/°C	m W				
dissipation MN74HC242S		Ta=-40~+60°C	D	275	m W				
	MIN/4HC2425	Ta=+60~+85°C	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m w				

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_O		0~Vcc	V
Operating temperature range	T _A		$-40 \sim +85$	°C
		2.0	0~1000	ns
Input rise and fall time	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

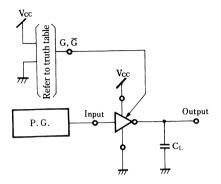
			Te	st Conditi	ons		Те	mperatu	ire		
Parameter	Symbol	V _{CC} (V)	Vı	Io		,	Γa = 25 °	2	Ta=-40)~+85°C	Unit
		(V)	,,	10	Unit	min.	typ.	max.	mın.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μ A	4.4	4.5		4.4	}	
Output HIGH voltage	Vон	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	V _{fL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36		İ	5.26		
		2.0		20.0	μΑ		0.0	0.1		0.1	
		4.5	VIH	20.0	μA	ļ	0.0	0.1	}	0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μ A		0.0	0.1		0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μΑ
3-state output off state	T	6.0	$V_I = V$	IH or V	IL			+0.5		+50	
current	Ioz	6.0	$V_0 = V$	lcc or C	GND			± 0.5		±5.0	μ A
Quiescent supply current	$I_{\rm CC}$	6.0	$V_I = V_C$	c or GNI	$I_0 = 0$			8.0		80.0	μA



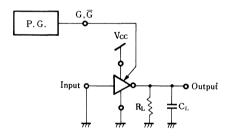
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

					Te	mperatu	re	Ĭ	
Parameter	Symbol	V _{CC} (V)	Test Conditions	,	Ta=25 °)	Ta=-40)~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13		16	
		2.0				50		65	
Output fall time	t THL	4.5			6	10		13	ns
		6.0				9		11	
D		2.0				75		95	
Propagation time	t _{PLH}	4.5			8	15		19	ns
$A \rightarrow B (L \rightarrow H)$		6.0				13		16	
Propagation time		2.0				75		95	
A→B (H→L)	t _{PHL}	4.5		į.	8	15		19	ns
$A \rightarrow B \ (\Pi \rightarrow L)$		6.0				13		16	
D		2.0				75		95	
Propagation time	t PLH	4.5			8	15		19	ns
$B \rightarrow A (L \rightarrow H)$		6.0				13		16	
Duono mation time	t _{PHL}	2.0				75		95	
Propagation time		4.5			8	15		19	ns
$B \rightarrow A (H \rightarrow L)$		6.0				13	1	16	
3-state propagation time		2.0				150		190	
	t PHZ	4.5	$R_L = 1 k\Omega$		17	30		38	ns
(H→Z)		6.0				26		33	
9 -1-1		2.0				125		155	
3-state propagation time	t PLZ	4.5	$R_L = 1 k\Omega$		15	25		31	ns
(L→Z)		6.0				21		26	
0.44		2.0				100		125	
3-state propagation time	t _{PZH}	4.5	$R_L = 1 k\Omega$		13	20		25	ns
(Z→H)		6.0				17		21	
2 -1-1		2.0				125		155	
3-state propagation time	t PZL	4.5	$R_L = 1 k\Omega$		15	25		31	ns
(Z→L)		6.0				21		26	

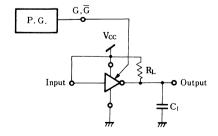
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , p_{LH} $t_{PHL}(A \rightarrow B \text{ or } B \rightarrow A)$
 - 1. Measuring Circuit

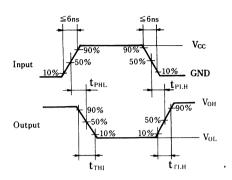


- (2) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit

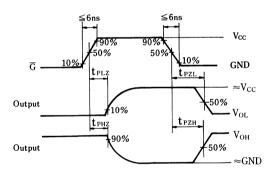


- [3] t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit





2. Waveforms



2. Waveforms

See above [2] 2. for waveforms.



MN74HC243/MN74HC243S

Quad TRI-STATE Transceivers

■ Description

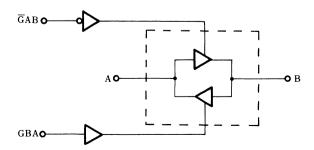
MN74HC243/MN74HC243S are high-speed tri-state output and non-inverted buffer transferring input bi-directionally and asynchronously through a data bus line. High-speed operation can be obtained for driving a large-capacity bus line due to large current output. It has input GBA where output A becomes enabled at HIGH, and input GAB where output B becomes enable at LOW. Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

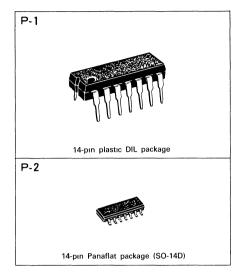
■ Truth Table

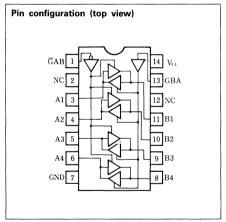
Contro	l Inputs	Data Port Status				
GAB	GBA	A	В			
Н	Н	Output	Input			
L	Н	*	*			
Н	L	Hi-Z	Hi-Z			
L	L	Input	Output			

Note

- 1. *: If transceiver is bi-directionally at the same time, destructive oscillation may be generated.
- 2. Hi-Z: High impedance







	Paramete	r	Symbol	Rating	Unit	
Supply volta	ge		Vcc	-0.5~+7.0	V	
Input/output	voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V	
Input protec	tion diode current		I _{IK}	±20	mA	
Output paras	sitic diode current		Іок	± 20	mA	
Output current			Io	±35	mA	
Supply curre	ent		Icc, Igyd	±70	mA	
Storage temp	perature range		Tstg	-65~+150	C	
Allar.	MN74HC243	Ta=-40~+60°C	P_{D}	400	m W	
Power	$T_0 = \pm 60 - \pm 95\%$		F ()	Decrease to 200mW at the rate of 8mW/°C	III VV	
dissipation	dissipation MN74HC243S $Ta=-40\sim+60^{\circ}$ C		ъ	275	11/	
	WIN/4HC2435	$T_a = +60 \sim +85 ^{\circ}$	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m W	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	T _A		-40~+85	c
		2.0	0~1000	ns
Input rise and fall time	t_r, t_f	4.5	0~500	ns
		6.0	0~400	ns

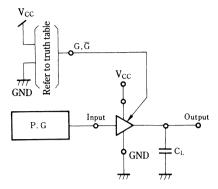
			Te	Test Conditions			Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Vı	Io			Ta=25°	2	$T_a=-40$)~+85℃	Unit
		(- /	•1	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15	l		3.15		v
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	VIL	4.5					ļ	0.9		0.9	v
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	Vон	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1	1	0.1	V
		4.5	VIL	6.0	mA			0.32)	0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	T	6.0	$V_I = V$	IH or V	IL			+0.5		+5.0	
current	Ioz	0.0	$V_0 = V$	cc or C	GND			± 0.5		±5.0	μΑ
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GNI	$I_0=0$			8.0		80.0	μA



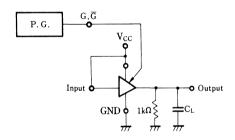
■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

					Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°		Ta=-40)~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			7	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				100		125	
	t _{PLH}	4.5			8	20		25	ns
$A \rightarrow B (L \rightarrow H)$		6.0				17		21	
Propagation time		2.0				100		125	
	t _{PHL}	4.5			6	20		25	ns
$A \rightarrow B (H \rightarrow L)$		6.0				17		21	
D		2.0				100		125	
Propagation time	t _{PLH}	4.5			8	20		25	ns
$B \rightarrow A (L \rightarrow H)$		6.0				17		21	
Propagation time		2.0				100		125	
• •	t PHL	4.5			7	20		25	ns
$B \rightarrow A (H \rightarrow L)$		6.0				17		21	
		2.0				125		155	
3-state propagation time	t PHZ	4.5	$R_L = 1 k\Omega$		15	25		31	ns-
(H→Z)		6.0				21		26	
0		2.0				100		125	
3-state propagation time	t _{PLZ}	4.5	$R_L = 1 k\Omega$		12	20		25	ns
(L→Z)		6.0				17		21	
0 4 4		2.0				100		125	
3-state propagation time	t _{PZH}	4.5	$R_L = 1 k\Omega$		9	20		25	ns
(Z→H)		6.0				17		21	
3-state propagation time		2.0				100		125	
3-state propagation time (Z→L)	t PZL	4.5	$R_L = 1 k\Omega$		10	20		25	ns
(∠→∟)		6.0				17		21	

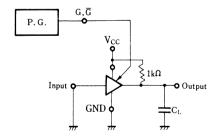
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , t_{PLH}/t_{PHI} (A \rightarrow B or B \rightarrow A)
 - 1. Measuring Circuit

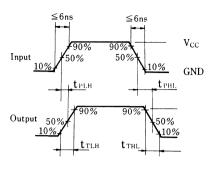


- (2) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit

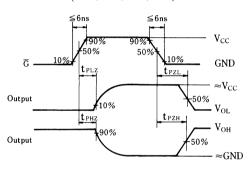


- (3) t_{PLZ}, t_{PZL}
 - 1. Measuring Circuit





2. Waveforms (tphz, tpzh, tplz, tpzl)





MN74HC244/MN74HC244S

Octal TRI-STATE Buffers

■ Description

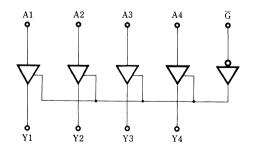
MN74HC244/MN74HC244S are high-speed non-inverted buffers consisting of octal tri-state outputs. High-speed operation is possible for driving a large capacitance bus line owing to large current output. Inputs $1\overline{G}$ and $2\overline{G}$ are available where output becomes enabled at LOW, and each input controls 4 buffers. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

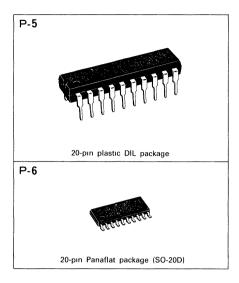
■ Truth Table

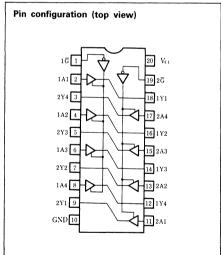
Ing	out	Output	In	put	Output
1Ğ	1 A	1 Y	2 G	2 A	2 Y
L	L	L	L	L	L
L	Н	Н	L	Н	Н
Н	L	Hi-Z	Н	L	Hi-Z
Н	Н	Hi-Z	Н	Н	Hi-Z

Note:

1. Hi-z: High impedance







	Paramete	er	Symbol	Rating	Unit	
Supply voltage	ge		$V_{\rm CC}$	-0.5∼+7.0	v	
Input/output	voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V	
Input protec	tion diode current		I _{IK}	±20	mA	
Output paras	sitic diode current		Іок	±20	mA	
Output current			Io	± 35	mA	
Supply curre	ent		Icc, IGND	±70	mA	
Storage tem	temperature range		Tstg	-65~+150	${\mathbb C}$	
	MN74HC244	Ta=-40~+60°C	P_{D}	400	m W	
Power	Power $T_a = +60 \sim +85 ^{\circ}$		F J)	Decrease to 200mW at the rate of 8mW/°C	m w	
dissipation	Issipation MN74HC244S $Ta = -40 \sim +60 \text{°C}$		ъ	275		
	$T_a = +60 \sim +85 \%$		Po	Decrease to 200mW at the rate of 3.8mW/°C	m W	

■ Operating Conditions

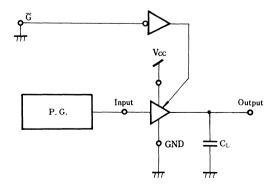
Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	v
Input/output voltage	V_{I}, V_{O}		0~V _{CC}	v
Operating temperature range	TA		-40~+85	C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

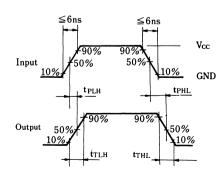
			Tes	t Conditio	ns	1	Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Vı	Io		•	Γa=25 °	0	Ta=-40)~+ 85 ℃	Unit
			٧١	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5		,	1.5		
Input HIGH voltage	V_{1H}	4.5				3.15			3.15		V
		6.0				4.2		İ	4.2		
		2.0						0.3		0.3	
Input LOW voltage	VIL	4.5	İ					0.9		0.9	V
		6.0	İ					1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	ViH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	Vон	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V _{fL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1	ŧ	0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	Ioz	6.0	$V_I = V$	THOR V	IL			±0.5		±5.0	μA
current	IOZ	0.0	$V_0 = V$	or C	GND					±3.0	μα
Quiescent supply current	I_{CC}	6.0	$V_1 = V_0$	cc or GNI	$I_0=0$			8.0		80.0	μΑ

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

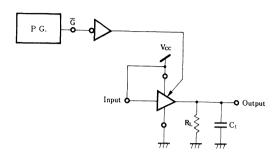
					Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25 °	2	Ta=-40)~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0			18	75		95	
Output rise time	t _{TLH}	4.5			9	15		19	ns
		6.0				13		16	
		2.0			17	75		95	
Output fall time	t _{THL}	4.5			8	15		19	ns
		6.0				13		16	
T		2.0			16	75		95	
Propagation time	t _{PLH}	4.5		ļ	8	15		19	ns
(L→H)		6.0	•			13		16	
		2.0			18	75		95	
Propagation time	t PHL	4.5			8	15		19	ns
(H→L)		6.0				13		16	
2 -4-4		2.0			21	125		155	
3-state propagation time	t _{PHZ}	4.5	$R_L = 1 k\Omega$		13	25		31	ns
(H→Z)		6.0				21	1	26	
		2.0			28	125		155	
3-state propagation time	t _{PLZ}	4.5	$R_L = 1 k\Omega$		16	25		31	ns
(L→Z)		6.0				21	1	26	
		2.0			25	100		125	
3-state propagation time (Z→H)	t _{PZH}	4.5	$R_L = 1 k\Omega$		12	20	ļ	25	ns
		6.0				17		21	
2 -1-1		2.0			33	125		155	
3-state propagation time	t _{PZL}	4.5	$R_L = 1 k\Omega$		14	25		31	ns
(Z→L)		6.0				21		26	

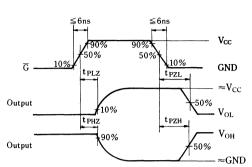
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , t_{PLH} , t_{PHL}
 - 1. Measuring Circuit





- (2) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit

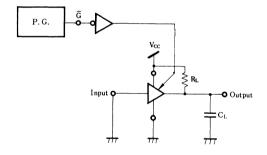




- [3] t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit

2. Waveforms

See above [2] 2. for waveforms.





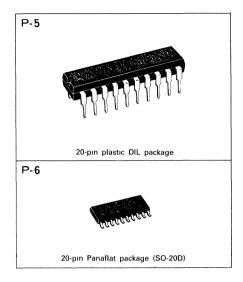
MN74HC245/MN74HC245S

Octal TRI-STATE Transceivers

■ Description

MN74HC245/MN74HC245S are high-speed non-inverted bidirectional buffers consisting of octal tri-state output. Input is transferred bi-directionally asynchronously through a data bus line. Large current output enables high-speed operation for driving a large capacitance bus line. It has input G where output becomes enabled at LOW, and direction control input DIR. When DIR input is HIGH, data is transferred from input A to B, and, when DIR input is LOW, data is transferred from input B to output A. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs are directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

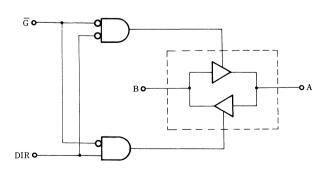


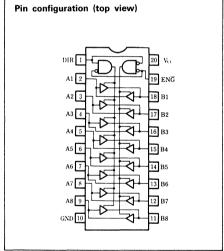
■ Truth Table

Enable G	Direction Control DIR	Operation
L	L	B data to A bus
L	Н	A data to B bus
Н	×	Hi-Z

Note:

- 1. Hi-Z: High impedance
- 2. × Either HIGH OR LOW; it doesn't matter





	Parameter		Symbol	Rating	Unit																
Supply volta	age		ge		oltage		voltage		ply voltage		oly voltage		ge		Vcc	$-0.5 \sim +7.0$	V				
Input/output	t voltage		t/output voltage		ut/output voltage		ıt voltage		utput voltage		put voltage		voltage		t voltage		itput voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	ction diode current		I_{1K}	± 20	mA																
Output paras	sitic diode current		Іок	±20	mA																
Output curre	ent		Io	± 35	mA																
Supply curre	ent		Icc, IGND	±70	mA																
Storage tem	perature range		Tstg	$-65 \sim +150$	°C																
	MN74HC04F	$T_a = -40 \sim +60 \text{°C}$	P_{D}	400	117																
Power	Power MN74HC245 $T_a = +60 \sim +85 ^{\circ}$ C		(F))	Decrease to 200mW at the rate of 8mW/°C	mW																
dissipation	MN74HC245S 1a-40~+00C		D	275	W																
	MIN74HC2455	$T_a = +60 \sim +85 ^{\circ}$	Po	Decrease to 200mW at the rate of 3.8mW/°C	m W																

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	T _A		$-40 \sim +85$	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

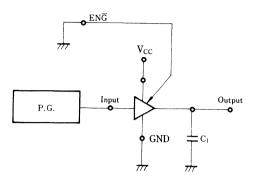
			Test Conditions		Temperature						
Parameter	Symbol	Vcc (V)	V_1	Io			Γa=25°	C	Ta=-40	0~+85℃	Unit
		(, ,		1()	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0		}		4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	Vih	-20.0	μA	4.4	4.5	r	4.4		
Output HIGH voltage	Von	6.0	or	-20.0	μ A	5.9	6.0	1	5.9		V
		4.5	V _{II} .	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36		}	5.26		
		2.0		20.0	μΑ		0.0	0.1		0.1	
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	T	6.0	$V_1 = V$	IH or V	IL.			+0.5		+50	
current	Ioz	0.0	Vo=Vcc or GND				± 0.5		±5.0	μΑ	
Quiescent supply current	$I_{\rm CC}$	6.0	$V_1 = V_0$	c or GNI	$I_0 = 0$			8.0		80.0	μA

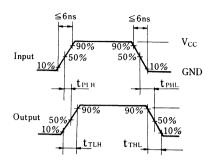


■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

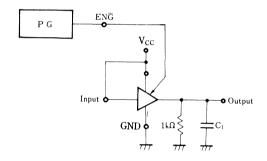
					Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°		Ta=-40)~+85℃	Unit
		(,,		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5		}	7	15		19	ns
		6.0		1		13		16	
		2.0				75	,	95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
D		2.0				75		95	
Propagation time	t _{PLH}	4.5			5	15		19	ns
(L→H)		6.0				13		16	
D		2.0				75		95	
Propagation time (H→L)	t _{PHL}	4.5			5	15		19	ns
(H→L)		6.0				13		16	
2 -4-4-		2.0				150		190	
3-state propagation time	t PHZ	4.5	$R_L = 1 k\Omega$		16	30		38	ns
(H→Z)		6.0				26	į	33	
3-state propagation time		2.0				150		190	
	t _{PLZ}	4.5	$R_L = 1 k\Omega$		18	30		38	ns
(L→Z)		6.0				26		33	
3-state propagation time		2.0				100		125	
	t _{PZH}	4.5	$R_L = 1 k\Omega$		12	20		25	ns
(Z→H)		6.0				17		21	
0 11		2.0				125		155	
3-state propagation time	t PZL	4.5	$R_L = 1 k\Omega$		14	25		31	ns
(Z→L)		6.0				21		26	

- Switching Time Measuring Circuit and Waveforms
- (1) ttlh, tthl, tplh, tphl
 - 1. Measuring Circuit

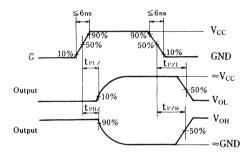




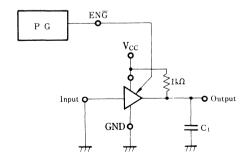
- (2) tpHz, tpZH
 - 1. Measuring Circuit



2. Waveforms $(t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})$



- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit



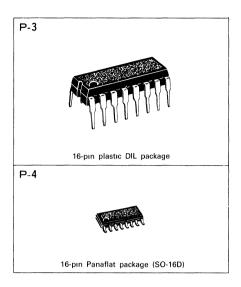
MN74HC251/MN74HC251S

8-Channel TRI-STATE Multiplexer

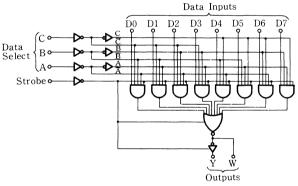
■ Description

MN74HC251/MH74HC251S are 8-channel tri-state multiplexer selecting one input from eight channel data input; each multiplexer has a reverse phase output Y, W, and strobe input. When strobe input is "L", the circuit becomes enabled; when strobe input is "H", status. Accordingly, when strobe input is "L", one input is selected according to the select input A, B, C combination, and data is transferred to outputs Y, W.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

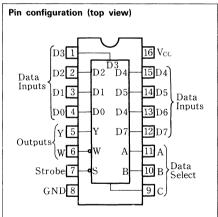


■ Logic Diagram



■ Truth Table

	Inp	ut		Out	put
	Select		Strobe	Y	W
С	В	A	Strobe	1	VV
×	×	×	Н	Hi-Z	Hi-Z
L	L	L	L	D0	$\overline{\mathrm{D0}}$
L	L	Н	L	D1	$\overline{\mathrm{D1}}$
L	Н	L	L	D2	$\overline{\mathrm{D2}}$
L	Н	Н	L	D3	$\overline{\mathrm{D3}}$
Н	L	L	L	D4	$\overline{\mathrm{D4}}$
Н	L	Н	L	D5	$\overline{\mathrm{D5}}$
Н	Н	L	L	D6	$\overline{\mathrm{D6}}$
Н	Н	Н	L	D7	D7



- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance
- 3. D0, D1, D7: Related D input level

	Parameter		Symbol	Rating	Unit													
Supply volta	Supply voltage			oltage		age		tage		oltage		voltage		ply voltage		Vec	$-0.5 \sim +7.0$	V
Input/output	ut/output voltage		utput voltage		t voltage		V_{I}, V_{O}	$-0.5 \sim V_{(c)} + 0.5$	V									
Input protec	tion diode current		I_{lk}	± 20	mA													
Output para	sitic diode current		Iok	±20	mA													
Output curre	ent		Ιο	± 25	mA													
Supply curre	ent		Icc, Iond	± 50	mA													
Storage tem	perature range		Tstg	-65~+150	°C													
	MN74HC251	Ta=-40~+60℃	P_{D}	400	m W													
Power	Power $Ta = +60 \sim +85 ^{\circ}$		I I D	Decrease to 200mW at the rate of 8mW/°C	III VV													
dissipation	MN74HC251S 1a-40~+00C		D.	275	W													
	MIN74HC2515	Ta=+60~+85°C	P_{b}	Decrease to 200mW at the rate of 3.8mW/°C	m W													

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vec		$1.4 {\sim} 6.0$	V
Input/output voltage	V_1, V_0		0~V(c	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

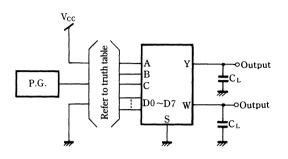
		V	Tes	st Conditio	ons		Те	mperatu	re		
Parameter	Symbol	V66 (V)	Vı	Io		,	Γa=25 °	C	Ta=-40)~+85 ℃	Unit
			V 1	207	Unit	mın.	typ.	max.	mın.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	Vih	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	VIL	4.5						0.9	1	0.9	V
		6.0						1.2		1.2	
	i	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	ViH	-20.0	μA	4.4	4.5	ļ	4.4		
Output HIGH voltage	Vон	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	Víi	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μΑ		0.0	0.1		0.1	
		4.5	V_{IH}	20.0	μA		0.0	0.1	l	0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1	ı	0.1	V
		4.5	VII	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	T	6.0	$V_I = V$	IH or V	II.			+0.5		+50	
current	Ioz	$V_0 = V_{CC}$ or GND				± 0.5		± 5.0	μ A		
Quiescent supply current	Ic.	6.0	$V_1 = V_0$.c or GNI	$I_0=0$			8.0		80.0	μΑ



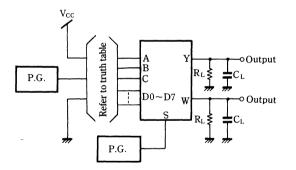
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

					Te	mperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Ta=25 ℃	2	Ta=-40)~+85°C	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0		1		13		16	
Propagation time		2.0				150		190	
$D \rightarrow Y$, $W(L \rightarrow H)$	t _{PLH}	4.5				30		38	ns
D→1, W(L→n)		6.0				26		33	
D		2.0				150		190	
Propagation time $D \rightarrow Y$, $W(H \rightarrow L)$	t PHL	4.5				30		38	ns
$D \rightarrow Y, W(H \rightarrow L)$		6.0		1		26		33	
Propagation time		2.0				150		190	
A,B,C \rightarrow Y,W(L \rightarrow H)	t _{PLH}	4.5				30		38	ns
A, B, C→ 1, W (L→ H)		6.0				26		33	
Propagation time	t _{PHL}	2.0				150		190	
A, B, $C \rightarrow Y$, W ($H \rightarrow L$)		4.5				30		38	ns
$A, B, C \rightarrow I, W (\Pi \rightarrow L)$		6.0				26		33	
3-state propagation time		2.0				100		125	
(H→Z)	t PHZ	4.5	$R_{L}=1k\Omega$			20		25	ns
(n→Z)		6.0			1	17	l	21	
3-state propagation time		2.0				100		125	
(L→Z)	t _{PLZ}	4.5	$R_L = 1k\Omega$			20		25	ns
(L→Z)		6.0				17		21	
3 state propagation time		2.0				100		125	
3-state propagation time	t _{PZH}	4.5	$R_L = 1k\Omega$	1		20		25	ns
(Z→H)		6.0				17		21	
s-state propagation time		2.0				100		125	
	t _{P71}	4.5	$R_{I.}=1k\Omega$			20		25	ns
(Z→L)		6.0				17		21	

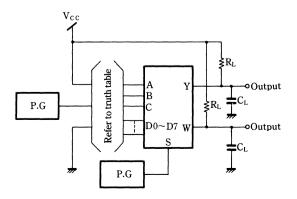
- Switching Time Measuring Circuit and Waveforms
- (1) ttlh, tthl, tplh, tphl
 - 1. Measuring Circuit

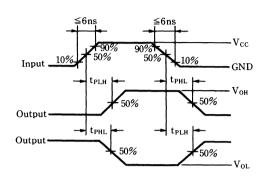


- (2) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit

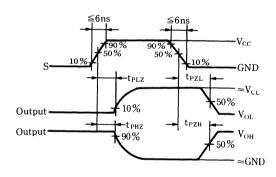


- (3) t_{PLZ}, t_{PZL}
- 1. Measuring Circuit





2. Waveforms



2. Waveforms

See above [2] 2. for waveforms.



MN74HC253/MN74HC253S

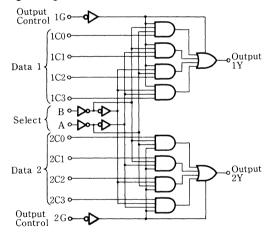
Dual 4-Channel TRI-STATE Multiplexers

■ Description

MN74HC253/MH74HC253S contain two tri-state multiplexers selecting one input from 4-channel data inputs in one chip. Output control input controls dual 4 lines respectively. When output control input is "H", output becomes high impedance regardless of bus line. When output control input is "L", data is transferred to the output by selecting output channel suited for data input signal from select input A and B.

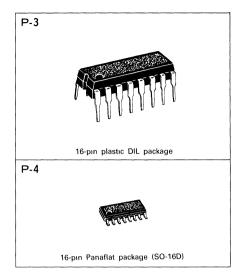
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

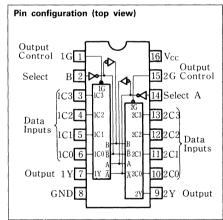
■ Logic Diagram



■ Truth Table

	Input										
Sel	ect	Data				Output Control	Output				
В	A	C0	C1	C 2	С3	G	Y				
×	×	×	×	×	×	Н	Hi-Z				
L	L	L	×	×	×	L	L				
L	L	Н	×	×	×	L	Н				
L	Н	×	L	×	×	L	L				
L	Н	×	Н	×	×	L	Н				
Н	L	×	×	L	×	L	L				
Н	L	×	×	Н	×	L	Н				
Н	Н	×	×	×	L	L	L				
Н	Н	×	×	×	Н	L	Н				





Note

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. H₁-Z: H₁gh impedance

	Parameter			Rating	Unit		
Supply voltag	ge		Vcc	Vcc -0.5~+7.0			
Input/output	ut voltage		utput voltage		V ₁ , V ₀	$-0.5 \sim V_{CC} + 0.5$	V
Input protection diode current			I_{1K}	± 20	mA		
Output parasitic diode current			Iok	± 20	mA		
Output curre	ıt		Io	± 25	mΑ		
Supply curre	ent		Icc, IGND	±50	mA		
Storage tem	perature range		Tstg	-65~+150	${\mathbb C}$		
	MNZALICOFO	Ta=-40~+60°C	D	400	11/		
Power	MN74HC253	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	m W				
dissipation	MN74HC9E2C	Ta=-40~+60℃	D.	275	m W		
	MN74HC253S	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m vv		

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V,
Input/output voltage	V_{I}, V_{O}		0~Vcc	V
Operating temperature range	T_{A}		-40~+85	℃
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

			Test Conditions			Temperature					
Parameter	Symbol	V _{CC} (V)	V_1	I _o ,	2007	Ta=25℃			Ta=-40~+85°C		Unit
		(•)	•	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	Vон	4.5	Vih	-20.0	μA	4.4	4.5	ļ	4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{1L}	- 6.0	mA	3.86			3.76		
		6.0		- 7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	ViH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	6.0	mA			0.32		0.37	
		6.0		7.8	mA	1		0.32		0.37	
Input current	II	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	Ioz	I _{OZ} 6.0	$V_I = V_{IH} \text{ or } V_{IL}$ $V_O = V_{CC} \text{ or GND}$				±0.5		±5.0	Λ	
current										μΑ	
Quiescent supply current	$I_{\rm CC}$	6.0	$V_I = V_C$	c or GNI), $\overline{I_0}=0$			8.0		80.0	μA

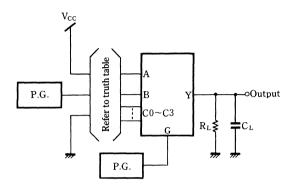


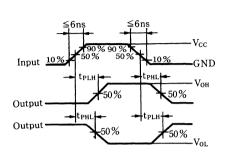
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

					Te	mperat	ure		
Parameter	Symbol	V _{CC} (V)	7Test Conditions		Ta=25 °	2	Ta=-40)~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				150		190	
	t PLH	4.5			18	30		38	ns
$A,B \rightarrow Y(L \rightarrow H)$		6.0				26		33	
Propagation time		2.0				150		190	
A,B→Y(H→L)	t _{PHL}	4.5			17	30		38	ns
$A, B \rightarrow I (H \rightarrow L)$		6.0				26		33	
Propagation time	t _{PLH}	2.0				150		190	
Propagation time $C \rightarrow Y(L \rightarrow H)$		4.5			18	30		38	ns
$C \rightarrow I (L \rightarrow H)$		6.0				26		33	
Propagation time	t _{PHL}	2.0				150		190	
$C \rightarrow Y (H \rightarrow L)$		4.5			17	30		38	ns
C→I (H→L)		6.0				26		33	
3-state propagation time		2.0				125		155	
3-state propagation time (H→Z)	t PHZ	4.5	$R_L=1k\Omega$		12	25		31	ns
(n→ Z)		6.0			ļ	21		26	
3-state propagation time		2.0				125		155	
(L→Z)	t PLZ	4.5	$R_L=1k\Omega$		13	25		31	ns
(L→Z)		6.0				21		26	
2 atata propagation time		2.0				150		190	
3-state propagation time (Z→H)	t _{PZH}	4.5	$R_L=1k\Omega$		17	30		38	ns
		6.0				26		33	
3-state propagation time		2.0				100		125	
3-state propagation time (Z→L)	t PZL	4.5	$R_L=1k\Omega$		10	20		25	ns
(Z¬L)		6.0				17		21	

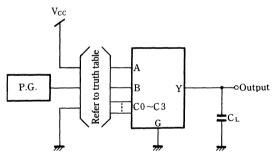
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH}, t_{THL}, t_{PLH}. t_{PHL}
 - 1. Measuring Circuit

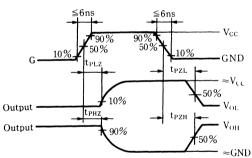




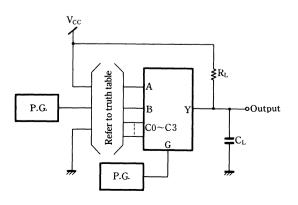


- (2) t_{PHZ}, t_{PZH}
 - 1. Measuring Circuit





- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.



MN74HC257/MN74HC257S

Quad 2-Channel TRI-STATE Multiplexers

■ Description

MN74HC257/MH74HC257S contain four tri-state multiplexers selecting one input from two data inputs in one chip. Input is composed of two data inputs A, B each determining the output, output control, and select input common to four output groups. When output control is "H", quad multiplexer outputs become high impedance. If select input is "H" at LOW level, data B status is output; if select input is "L", data A status is output. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

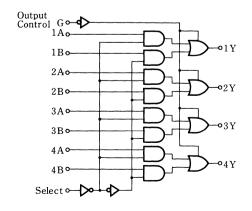
■ Truth Table

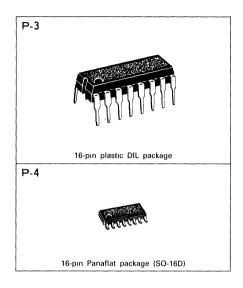
	Output			
G	Select	A	В	Y
Н	×	×	×	Hi-Z
L	L	L	×	L
L	L	Н	X	Н
L	Н	×	L	L
L	Н	×	Н	Н

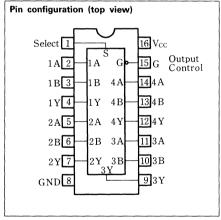
Note:

1. ×: Either HIGH or LOW; it doesn't matter

2. Hi-Z: High impedance







	Parameter			Rating	Unit								
Supply voltage	oltage		oltage		y voltage		pply voltage		Vcc	$-0.5 \sim +7.0$	V		
Input/output	out voltage		tput voltage		output voltage/		tput voltage		t/output voltage		$V_{\rm I},V_{\rm O}$	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	Input protection diode current			protection diode current		protection diode current		Iıк	±20	mA			
Output paras	Output parasitic diode current			±20	mA								
Output curre	Output current			±25	mA								
Supply curre	ent		Icc, IGND	± 50	mA								
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$ C								
	MN74HC257 Ta=−40~+60°C		Ta=-40~+60°C	400	m W								
Power	MN74HC257	Ta=+60~+85℃	$P_{\rm D}$	Decrease to 200mW at the rate of 8mW/°C	m w								
dissipation	• 1	Ta=-40~+60℃	D.	275	mW								
	MN74HC257S	Ta=+60~+85 ℃	Po	Decrease to 200mW at the rate of 3.8mW/°C	m vv								

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_{I}, V_{O}		0~Vcc	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r ,tf	4.5	0~500	ns
		6.0	0~400	ns

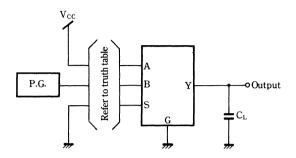
	.,		Test Conditions		Temperature						
Parameter	Symbol	(V)	V_1	I _O	Io		Ta=25℃			0~+85℃	Unit
		()	,,		Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5		Ì		3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	$V_{\rm IL}$	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	Vон	4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VII	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36		Ì	5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA	ļ	0.0	0.1		0.1	V
	:	4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_1	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	Ioz		$V_I = V_{IH} \text{ or } V_{IL}$ $V_O = V_{CC} \text{ or GND}$		IL			105		15.0	
current		6.0					± 0.5		±5.0	μA	
Quiescent supply current	$I_{\rm CC}$	6.0	$V_I = V_C$	c or GNI), $I_0=0$			8.0		80.0	μA

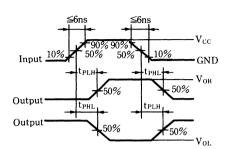


■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

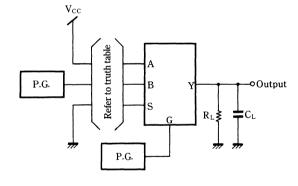
					Te	mperatı	ıre		Unit
Parameter	Symbol	Vcc	Test Conditions	•	Ta=25°C	;	Ta=-40	~+85℃	
		(V)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13	l	16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15	1	19	ns
		6.0				13	Ì	16	
D .: .:		2.0				150		190	
Propagation time	t _{PLH}	4.5			13	30	1	38	ns
$A,B\rightarrow Y (L\rightarrow H)$		6.0		1		26		33	
D		2.0				150		190	
Propagation time	t _{PHL}	4.5			12	30		38	ns
$A,B \rightarrow Y (H \rightarrow L)$		6.0				26		33	
D		2.0				150		190	
Propagation time	t _{PLH}	4.5			13	30		38	ns
$S \rightarrow Y (L \rightarrow H)$		6.0				26	{	33	
		2.0				150		190	
Propagation time	t _{PHL}	4.5]	13	30		38	ns
$S \rightarrow Y (H \rightarrow L)$		6.0				26	Ì	33	
		2.0				125		155	
3-state propagation time	t PHZ	4.5	$R_{L}=1k\Omega$	1	12	25		31	ns
(H→Z)		6.0		1	}	21		26	
		2.0				125		155	
3-state propagation time	t PLZ	4.5	$R_{1}=1k\Omega$		13	25	ļ	31	ns
(L→Z)		6.0			l	21		26	
3-state propagation time (Z→H)		2.0				100		125	
	t PZH	4.5	$R_L=1k\Omega$		10	20		25	ns
		6.0				17		21	
2 -1-1		2.0				100		125	
3-state propagation time	t PZL	4.5	$R_{i.}=1k\Omega$		10	20		25	ns
(Z→L)		6.0				17		21	

- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}
 - 1. Measuring Circuit

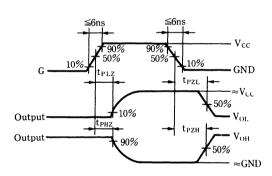




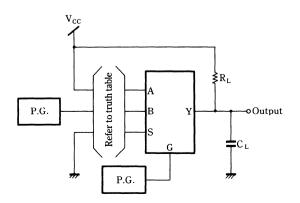
- (2) t_{PHZ}, t_{PZH}
 - 1. Measuring Circuit



2. Waveforms



- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.



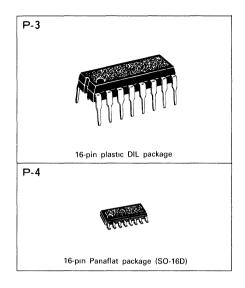
MN74HC258/MN74HC258S

Quad 2-Channel TRI-STATE Multiplexers (Inverted Output)

■ Description

MN74HC258/MH74HC258S contain four tri-state multiplexers selecting one input from two data inputs in one chip. Input is composed of two data inputs A, B each determining the output, output control, and select input common to four output groups. When output control is "H", quad multiplexer outputs become high impedance. If select input is "H" inverted data B is output; if select inputs is "L", inverted data A is output.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

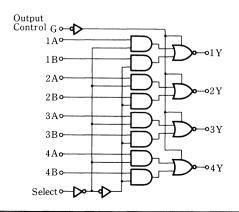


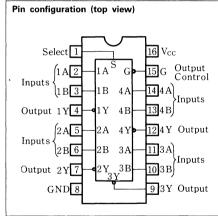
■ Truth Table

	Input						
G	Select	A	В	Y			
Ή	×	×	×	Hi-Z			
L	L	L	×	Н			
L	L	Н	×	L			
L	Н	×	L	Н			
L	Н	×	Н	L			

Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance





	Paramete	r	Symbol	Rating	Unit									
Supply voltage	Supply voltage			oly voltage		voltage		voltage		oltage		Vcc	$-0.5 \sim +7.0$	V
Input/output	voltage		V_1, V_0	$-0.5 \sim V_{\text{C,C}} + 0.5$	V									
Input protec	Input protection diode current			±20	mA									
Output paras	Output parasitic diode current			± 20	mA									
Output curre	Output current			± 25	mA									
Supply curre	ent		Ice, Ignd	±50	mA									
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$									
	MN74HC258	Ta=-40~+60°C	D	400	mW									
Power	MIN74HC236	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 8mW/°C	III VV									
dissipation	MN74HC258S	Ta=-40~+60°C	D	275	117									
	WIN/4HC2385	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m W									

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

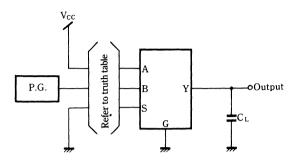
	17		Test Conditions			Te	mperati	ıre			
Parameter	Symbol	V _{CC} (V)	Vı	Io		,	Γa=25°	2	Ta=-40)~+85℃	Unit
		(•/	.,	10	Unit	mın.	typ.	max.	mın.	max.	
Input HIGH voltage		2.0				1.5			1.5		
	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V_{IH}	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	Vон	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	V_{fL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μ A		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μΑ		0.0	0.1		0.1	V
		4.5	y_{iL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	II	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	I	6.0	V _I =V _{IH} or V _{IL} V _O =V _{CC} or GND				+0.5		+5.0	μΛ	
current	Ioz	0.0					± 0.5		±5.0	μΑ	
Quiescent supply current	$I_{\rm CC}$	6.0	$V_I = V_C$.c or GNI	$I_0 = 0$			8.0		80.0	μA

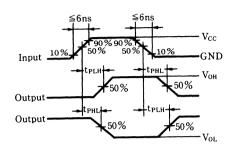


■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

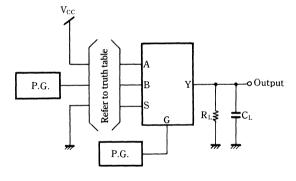
		37			Te	mperatu	ire		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25℃		Ta=-40)~+85℃	Unit
		(, ,		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15	Ì	19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13	1	16	
Propagation time		2.0				150		190	
	t PLH	4.5			12	30		38	ns
$A,B\rightarrow Y (L\rightarrow H)$		6.0				26		33	
		2.0				150		190	
Propagation time	t PHL	4.5			11	30		38	ns
$A,B\rightarrow Y (H\rightarrow L)$		6.0				26		33	
Propagation time		2.0				150		190	
	t PLH	4.5			14	30		38	ns
$S \rightarrow Y (L \rightarrow H)$		6.0				26		33	
D	-	2.0				150		190	
Propagation time	t PHL	4.5			13	30		38	ns
$S \rightarrow Y (H \rightarrow L)$		6.0				26		33	
		2.0				125		155	
3-state propagation time	t _{PHZ}	4.5	$R_L=1k\Omega$		12	25		31	ns
$(H \rightarrow Z)$		6.0				21		26	
_		2.0				125		155	
3-state propagation time	t _{PLZ}	4.5	$R_L = 1k\Omega$		14	25		31	ns
$(L \rightarrow Z)$		6.0				21		26	
2 -4-4		2.0				100		125	
3-state propagation time	t _{PZH}	4.5	$R_1 = 1k\Omega$		10	20		25	ns
(Z→ H)		6.0				17		21	
2 -4-4		2.0		1		100		125	
3-state propagation time	t _{PZL}	4.5	$R_1 = 1k\Omega$		11	20		25	ns
Z→L)		6.0				17		21	

- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , t_{PLH} , t_{PHL}
 - 1. Measuring Circuit

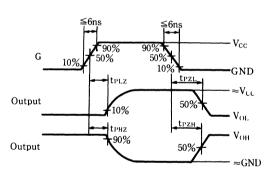




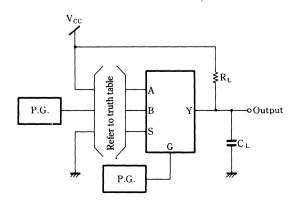
- (2) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit



2. Waveforms



- [3] t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.



MN74HC266/MN74HC266S

Quad 2-Input Exclusive NOR (XNOR) Gates

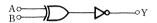
■ Description

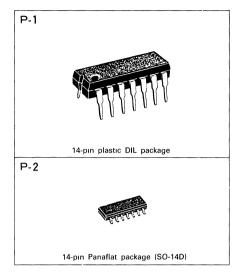
MN74HC266/MN74HC266S contain quad 2-input exclusive NOR gates.

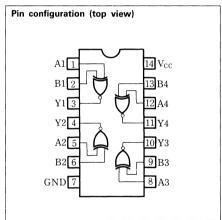
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic Diagram (1 gate)







■ Absolute Maximum Ratings

	Paramete	er	Symbol	Rating	Unit			
Supply volta	y voltage		ly voltage		$V_{\rm CC}$	-0.5~+7.0	V	
Input/output	voltage		V ₁ , V ₀	$-0.5 \sim V_{CC} + 0.5$	V			
Input protec	tion diode current		I_{1K}	±20	mA			
Output parasitic diode current			Іок	± 20	mA			
Output curre	Output current			put current		Io	±25	mA
Supply curre	current		Icc, I _{GND}	±50	mA			
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$			
	MN74HC266	Ta=-40~+60℃	P_{D}	400	mW			
Power	MN74fiC266	Ta=+60~+85°C	F))	Decrease to 200mW at the rate of 8mW/°C				
dissipation	MN74HC266S	Ta=-40~+60°C	D.	275	117			
	MN74HC2665	Ta=+60~+85°C	P _D	Decrease to 200mW at the rate of 3.8mW/°C	m W			

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	$V_{\rm I}, V_{\rm O}$		0~ Vcc	V
Operating temperature range	TA		$-40 \sim +85$	$^{\circ}$
		2.0	0~1000	ns
Input rise and fall time	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

- DC Gliaracteristics	(0.10	T	То	st Conditio	no		Т.				
<u></u>	0 1 1	V_{cc}	163	T				mperatu		1.0500	•••
Parameter	Symbol	(V)	$ v_i $	I ₀	Ta=25℃			Ta=-40~+85°C		Unit	
					Unit	mın.	typ.	max.	mın.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0		1		4.2		1	4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{IL}	4.5]				0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
	Vон	4.5	VIH	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V _{II} .	-4.0	mA	3.86		İ	3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μ A		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μ A		0.0	0.1		0.1	V
		4.5	V_{II}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μΑ
Quiescent supply current	Icc	6.0	$V_{\rm I} = V_{\rm O}$	c or GNI), I ₀ =0			2.0		20.0	μΑ

\blacksquare AC Characteristics (GND=0V, Input transition time ${\leq}6ns,~C_L{=}50pF)$

		.,	77		Temperature					
Parameter	Symbol	(V)	Test Conditions	Ta=25°C			Ta=-40~+85℃		Unit	
				mın.	typ.	max.	min.	max.		
		2.0			25	75		95		
Output rise time	t TLH	4.5			8	15		19	ns	
		6.0			7	13		16		
		2.0			20	75		95		
Output fall time	t _{THI.}	4.5			7	15		19	n_S	
		6.0			6	13		16		
		2.0			25	75		95		
Propagation time (L → H)	t _{PLH}	4.5			8	15		19	ns	
(2 11)		6.0			7	13		16		
D		2.0			25	75		95		
Propagation time $(H \rightarrow L)$	t PHL	4.5			8	15		19	ns	
		6.0			7	13		16		



MN74HC273/MN74HC273S

Quad D-Type Flip-Flops with Clear

Description

MN74HC273/MN74HC273S contain eight D-type flip-flops with clear. This is a master/slave flip-flop with common clock and clear. D input data satisfying set-up time is transferred to output Q on the positive-going edge of the clock pulse. When the clear input is low, all outputs are set to low. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs are directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

20-pin plastic DIL package P-6 20-pin Panaflat package (SO-20D)

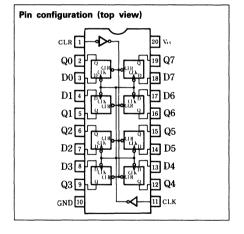
P-5

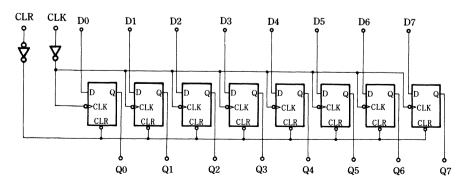
■ Truth Table

	Input							
CLR	CLK	D	Q					
L	×	×	L					
Н	5-	Н	Н					
Н	5	L	L					
Н	L	×	\mathbf{Q}_{O}					

Note:

- ____: Data Input is transmitted to output during the rise of clock from "L" to "H".
- 2. X₀: Either of "H" and "L" will do.
- 3. Q_0 : Q level before establishment of input conditions shown in the table.





Parameter			Symbol	Rating	Unit																
Supply voltag	y voltage		y voltage		y voltage		y voltage		ly voltage		Vec	-0.5∼+7.0	V								
Input/output	output voltage		output voltage		t/output voltage		ut/output voltage		output voltage		utput voltage		ut voltage		itput voltage		utput voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protection diode current			Iık	± 20	mA																
Output parasitic diode current			Іок	±20	mA																
Output curre	Output current			out current		out current		Io	±25	mA											
Supply curre	ly current		Icc, IGND	±50	mA																
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$																
	MN74HC273	$Ta = -40 \sim +60 \text{°C}$	$P_{\rm D}$	400	mW																
Power	MIN74HC273	Ta=+60~+85 °C	I ()	Decrease to 200mW at the rate of 8mW/°C	m vv																
dissipation	MN74HC273S	Ta=-40~+60℃	$P_{\rm D}$	275	117																
	141111111111111111111111111111111111111	Ta=+60~+85℃	F [)	Decrease to 200mW at the rate of 3.8mW/°C	m W																

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V _i ,V _o		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr,tf	4.5	0~500	ns
			0~400	ns

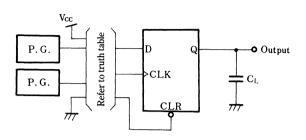
			Те	st Conditi	ons		Te	mperatu	re		
Parameter	Symbol	(V)	Vı	Io		•	Ta=25 °	C	Ta=-40	~+85℃	Unit
			V 1	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15		}	3.15		V
		6.0				4.2		;	4.2		
		2.0						0.3		0.3	
Input LOW voltage	VIL	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	Vон	4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GNI), I ₀ =0			8.0		80.0	μA



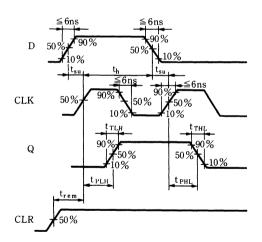
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

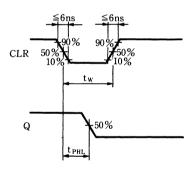
					Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Ta = 25 °C	2	Ta=-40	~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5		ł	8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t THL	4.5		l	6	15		19	ns
		6.0				13		16	
D +i		2.0				125		155	
Propagation time $CLK \rightarrow Q (L \rightarrow H)$	t PLH	4.5			12	25		31	ns
CLK→Q (L→H)		6.0				21		26	
Dunna mation time		2.0				125		155	
Propagation time	t PHL	4.5			13	25		31	ns
$CLK \rightarrow Q (H \rightarrow L)$		6.0				21		26	
D		2.0				125		155	
Propagation time	t PHL	4.5			14	25		31	ns
$CLR \rightarrow Q (H \rightarrow L)$		6.0				21		26	
		2.0				100		95	
Minimum Set-up time	t su	4.5			1	20		19	ns
		6.0]	1	17		16	
		2.0			_	0		0	
Minimum Hold time	th	4.5				0		0	ns
		6.0				0		0	
		2.0				100		125	
Minimum CLR pulse	t _w	4.5			6	20		25	ns
width		6.0				17		21	
		2.0				75		95	
Minimum recovery time	t _{rem}	4.5			2	15		19	ns
		6.0				13		16	
		2.0		6			4		
Maximum clock frequency	fmax	4.5		30	45		24		MHz
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit



 $\begin{aligned} \text{Waveforms-1} \left(& t_{TLH}, \ t_{THL}, \ t_{su}, \ f_{max}, \\ & t_{PLH}/t_{PHL}(CLK \rightarrow Q), \ t_{rem}, \ t_{h} \end{aligned} \right) & \text{Waveforms-2} \ \left(t_{PHL}(CLR \rightarrow Q), \ t_{w} \right) \end{aligned}$





MN74HC280/MN74HC280S

9-Bit Odd/Even Parity Generator/Checker

■ Description

MN74HC280/280S are 9-bit odd/even parity generator/checker, which have odd/even outputs to follow odd/even parity. Word length can be easily expanded by cascade connection.

All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2V or more is logic "1". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P- 1 14-pin plastic DIL package P- 2 14-pin Panaflat package (SO-14D)

14 Vcc

1315

Pin Configuration (top view)

17 16 15

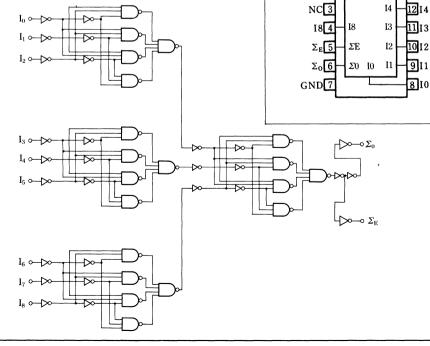
■ Truth Table

Input signal at HIGH level	Output			
from data input $(I_0 \sim I_8)$	ΣΕ	ΣΟ		
0, 2, 4, 6, 8 1, 3, 5, 7, 9	H L	L H		

Note:

1. H: HIGH level

2. L: LOW level



	Paramete	er	Symbol	Rating	Unit										
Supply voltag	Supply voltage			-0.5~+7.0	V										
Input/output	/oltage		voltage		voltage		voltage		ut voltage		put voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protect	ion diode current		I _{IK}	±20	mA										
Output parasi	tic diode current		I _{OK}	±20	mA										
Output curre	nt		I_{O}	±25	mA										
Supply curren	nt		I _{CC} , I _{GND}	±50	mA										
Storage temp	erature range		Tstg	−65~+150	°C										
	MN74HC280	Ta=-40~+60°C	P_{D}	400	mW										
Power			I FD	Decrease to 200mW at the rate of 8mW/°C	111 VV										
dissipation	MN74HC280S	Ta=-40~+60°C	р	275	mW										
	MIN74TC2805	Ta=+60~+85°C	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	IIIVV										

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0∼V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		V _{CC} =2.0V	0~1000	ns
Input rise and fall time	t _r , t _f	V _{CC} 4.5V	0~500	ns
		$V_{CC}=6.0V$	0~400	ns

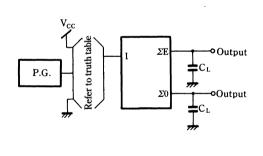
		V _{CC} (V)	Tes	t Condition	ons		T	emperatu	re	Ì]
Parameter	Symbol		Vı	,			Ta=25°C		Ta=-40	~+85°C	Unit
			V _I	I_{O}	Unit	mın.	typ.	max.	min.	max.	
		2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2	- 1	V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	v
		2.0		-20.0	μΑ	1.9	2.0		1.9		V
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		V
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V _{IL}	-4.0	mA	3.86			3.76		V
		6.0		-5.2	mA	5.36			5.26		V
		2.0		20.0	μA		0.0	0.1		0.1	v
		4.5	V _{IH}	20.0	μΑ		0.0	0.1		0.1	v
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1	,	0.1	V
		4.5	V _{IL}	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	Iı	6.0	V _I =	V _{CC} or G	ND			±0.1		±1.0	μA
Quiescent supply current	I _{CC}	6.0	$V_I = V_{CC}$	or GND	, I _O =0			8.0		80.0	μΑ



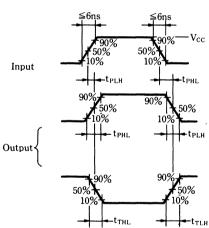
■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C_L=50pF)

					Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta=-40	~+85°C	Unit
		(,,		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5				15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5		1		15		19	ns
		6.0				13	Į	16	
Propagation time		2.0				150		190	
$I \rightarrow \Sigma E$	t _{PLH}	4.5		1	1	30		38	ns
(L→H)		6.0				30		38	
Propagation time		2.0				150		190	
I→ΣE	t _{PHL}	4.5				30	}	83	ns
(H→L)		6.0				26		33	
Propagation time		2.0				150		190	
I→ΣO	t _{PLH}	4.5				30		38	ns
(L→H)		6.0				26		33	
Propagation time $I \rightarrow \Sigma O$		2.0				150		190	
	t _{PHL}	4.5				30		38	ns
(H→L)		6.0			1	26		33	

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HCT280/MN74HCT280S

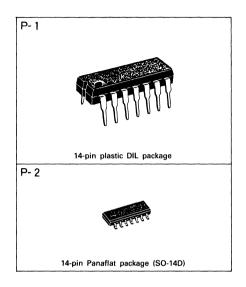
9-Bit Odd/Even Parity Generator/Checker (TTL Input)

■ Description

MN74HCT280/MN74HCT280S are 9-bit odd/even parity generator/checker, which have odd/even outputs to follow odd/even parity. Word length can be easily expanded by cascade connection.

All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2V or more is logic "1". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



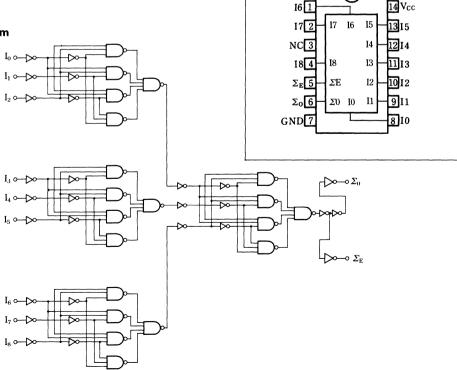
Pin Configuration (top view)

■ Truth Table

Input signal at HIGH level	Out	put
from data input (I ₀ ~I ₈)	ΣΕ	ΣΟ
0, 2, 4, 6, 8	Н	L
1, 3, 5, 7, 9	L	Н

Note:

1. H: HIGH level 2. L: LOW level





	Paramete	er	Symbol	Rating	Unit
Supply voltag	Supply voltage			-0.5~+7.0	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protect	ion diode current		I _{IK}	±20	mA
Output parasi	itic diode current		I _{OK}	±20	mA
Output curre	nt		I_{O}	±25	mA
Supply curren	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	erature range		Tstg	-65~+150	°C
	MN74HCT280	$Ta = -40 \sim +60^{\circ}C$	P_{D}	400	mW
Power	Power $Ta = +60 \sim +85^{\circ}C$		I D	Decrease to 200mW at the rate of 8mW/°C	111 VV
dissipation	MN74HCT280S	$Ta = -40 \sim +60^{\circ}C$	P_{D}	275	mW
	WIN 7411C 1 2005	Ta=+60~+85°C	r _D	Decrease to 200mW at the rate of 3.8mW/°C	11177

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		4.5~5.5	V
Input/output voltage	V _I , V _O		0∼V _{CC}	V
Operating temperature range	T _A	ļ	-40~+85	°C
Input rise and fall time	t _r , t _f	V _{CC} =4.5V	0~500	ns

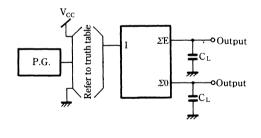
			Tes	t Condition	ons		T	emperatu	re		
Parameter ,	Symbol	V _{CC} (V)	V _I	I_{O}		Ta=25°C			Ta=-40	~+85°C	Unit
			VΙ	10	Unit	min.	typ.	max.	min.	max.	
		4.5									
Input HIGH voltage	V_{IH}	≀				2.0			2.0		V
		5.5									
		4.5									
Input LOW voltage	V_{IL}	≀						0.8		0.8	v
		5.5			ĺ						
		4.5	V_{IH}	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}		or					ĺ			V
		4.5	V _{IL}	-4.0	mA	3.86			3.76		V
		4.5	V _{IH}	20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	V_{OL}		or								V
		4.5	V _{IL}	4.0	mA			0.32		0.37	V
Input current	I _I	5.5	V _I =	V _{CC} or G	ND			±0.1		±1.0	μΑ
Quiescent supply current	I_{CC}	5.5	$V_I = V_{CC}$	or GND	, $I_0=0$			8.0		80.0	μΑ

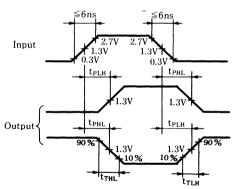
■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C_L=50pF)

					T	emperatu	re]
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta=-40	~+85°C	Unit
		(1)		min.	typ.	max.	min.	max.	
Output rise time	t _{TLH}	4.5				15		19	ns
Output fall time	t _{THL}	4.5				15		19	ns
Propagation time $I \rightarrow \Sigma E$ $(L \rightarrow H)$	t _{PLH}	4.5				30		38	ns
Propagation time $I \rightarrow \Sigma E$ $(H \rightarrow L)$	t _{PHL}	4.5				30		38	ns
Propagation time $I \rightarrow \Sigma O$ $(L \rightarrow H)$	t _{PLH}	4.5				30		38	ns
Propagation time $I \rightarrow \Sigma O$ $(H \rightarrow L)$	t _{PHL}	4.5				30		38	ns

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

2. Waveforms





MN74HC352/MN74HC352S

Dual 4-Input Multiplexers (Inverted Output)

■ Description

MN74H352/352S are dual 4-input multiplexers which transfer one of four inverted data to output Y according to the common select input (A, B). Each multiplexer has a respective strobe input. Multiplexer functions at LOW level. At HIGH level, output is fixed LOW.

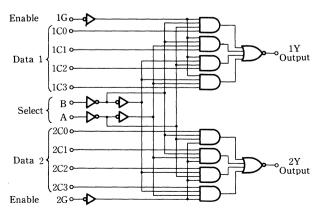
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directry driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

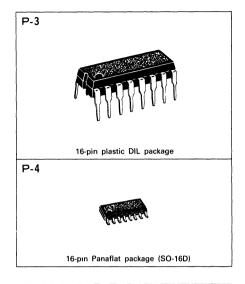
■ Truth Table

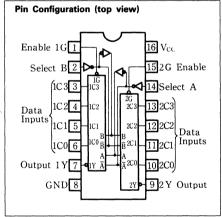
Select Inputs			Data 1	Inputs		Enable	Output
В	A	C0	C1	C2	СЗ	G	Y
×	×	×	×	×	×	Н	Н
L	L	L	×	×	×	L	Н
L	L	Н	×	×	×	L	L
L	Н	×	L	×	×	L	Н
L	Н	×	Н	×	×	L	L
Н	L	×	×	L	×	L	Н
Н	L	×	×	Н	×	L	L
Н	Н	×	×	×	L	L	Н
Н	Н	×	×	×	Н	L	L

Note:

1. ×: Either HIGH or LOW; it doesn't matter







	Parameter	r	Symbol	Rating	Unit				
Supply voltage	ge	:		-0.5∼+7.0	V				
Input/output	it voltage		it voltage		output voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	tion diode current		$I_{\rm IK}$	±20	mA				
Output paras	sitic diode current		Іок	±20	mA				
Output curre	ent		Io	±25	mA				
Supply curre	ent		Icc, IGND	±50	mA				
Storage tem	perature range		Tstg	-65~+150	${\mathbb C}$				
	MN74HC352	Ta=-40~+60°C	\mathbf{P}_{D}	400	mW				
Power	$T_2 = +60 \sim +85$		I	Decrease to 200mW at the rate of 8mW/°C	III VV				
dissipation	MN74HC352S	Ta=-40~+60℃	D.	275	mW				
	WIN1411C3525	Ta=+60~+85 ℃	Po	Decrease to 200mW at the rate of 3.8mW/°C	III VV				

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	$V_{\rm I}, V_{\rm O}$		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr,tf	4.5	0~500	ns
		6.0	0~400	ns

			Те	st Condit	ions	Temperature					
Parameter	Symbol	V _{cc} (V)	V _I	I ₀		Ta=25 ℃			Ta=-40)~+85 °C	Unit
		()	VI	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{II} .	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μA	5.9	6.0	ł	5.9		V
		4.5	V _{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	I _C c.	6.0	$V_I = V_C$	ι c or GNI	$I_0=0$			8.0		80.0	μA

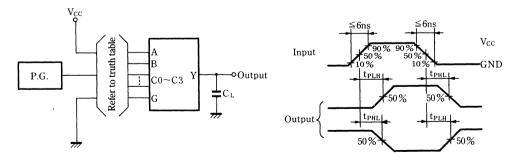


■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

		,,			Ter	nperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Γa=25 °C	2	Ta=-40	~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13	1	16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15	}	19	ns
		6.0				13	Ì	16	
		2.0				150		190	
Propagation time		4.5			18	30		38	ns
$A, B \rightarrow Y (L \rightarrow H)$	t _{PLH}	6.0				26		33	
D		2.0				150		190	
Propagation time	t PHL	4.5			17	30		38	ns
$A, B \rightarrow Y (H \rightarrow L)$	1	6.0				26		33	
Propagation time		2.0				150		190	
. 0	t PLH	4.5			17	30	į	38	ns
$G \rightarrow Y (L \rightarrow H)$		6.0				26		33	
D		2.0				150		190	
Propagation time	t PHL	4.5			17	30	Ì	38	ns
$G \rightarrow Y (H \rightarrow L)$		6.0				26		33	
D		2.0				175		220	
Propagation time	t PLH	4.5			19	35		44	ns
$C \rightarrow Y (L \rightarrow H)$		6.0				30		37	
D time time		2.0				175		220	
Propagation time	t PHL	4.5			20	35		44	ns
$C \rightarrow Y (H \rightarrow L)$		6.0				30		37	

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

2. Switching Waveforms



MN74HC353/MN74HC353S

Dual 4-Channel TRI-STATE Multiplexers (Inverted Output)

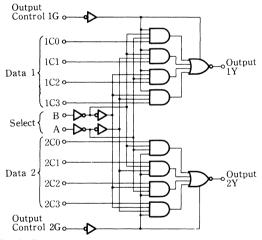
■ Description

MN74HC353/MH74HC353S contain dual 4-channel tri-state multiplexers (Inverted Output) in one chip, selecting one input from four channel data input. The output control input controls two sets of four lines respectively. When output control is "H", output becomes high impedance regardless of bus line. When output control input is "L", the output channel suited to the data input signal from select input A or B is selected, the data is inverted and transferred to the output.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

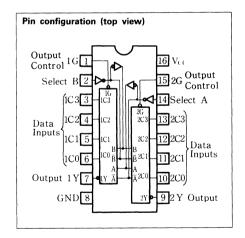
P-3 16-pin plastic DIL package P-4 16-pin Panaflat package (SO-16D)

■ Logic Diagram



■ Truth Table

			Inp	ut			0
Sel	lect		Da	ata		Output Control	Output
В	A	C0	C1	C2	СЗ	G	Y
×	×	×	×	×	×	Н	H1-Z
L	L	L	×	×	×	L	Н
L	L	Н	×	×	×	L	L
L	Н	×	L	×	×	L	Н
L	Н	×	Н	×	×	L	L
Н	L	×	×	L	×	L	Н
Н	L	×	×	Н	×	L	L
Н	Н	×	×	×	L	L	Н
Н	Н	×	×	×	Н	L	L



Note:

1. ×: Either HIGH or LOW; it doesn't matter

2. Hi-Z: High impedance

	Paramete	er	Symbol	Rating	Unit
Supply volta	oltage		$V_{\rm CC}$	-0.5~+7.0	V
Input/output	voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	tion diode current		I_{1K}	±20	mA
Output paras	sitic diode current		Ioĸ	±20	mA
Output curre	ent		Io	±25	mA
Supply curre	ent		Icc, IGND	±50	mA
Storage tem	perature range		Tstg	-65~+150	°C
	MN74HC353	Ta=-40~+60℃	Po	400	mW
Power	Power $Ta=+60\sim+3$		F ()	Decrease to 200mW at the rate of 8mW/°C	m w
dissipation	MN74HC353S	Ta=-40~+60℃	D.	275	m W
	WIN14HC3335	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m w

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		37	Test Conditions		ons	Temperature					
Parameter	Symbol	(V)	Vı	Io		Ta=25 ℃			Ta=-40)~+85 ℃	Unit
			''	10	Unit	mın.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
		4.5	Vih	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	Vil	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	Vih	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V _{II} .	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Ιı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	Ioz	6.0		TH or V				±0.5		±5.0	μΑ
current			$V_0 = V$	lec or (GND						,
Quiescent supply current	I_{CC}	6.0	$V_1 = V_0$	c or GNI	$I_0=0$			8.0		80.0	μA

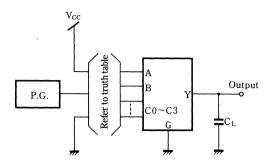
Panasonic -270-

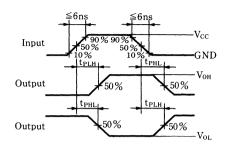
■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

		.,			Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Γa = 25°	2	Ta=-40	~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5		1	8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
D time		2.0				150		190	
Propagation time	t _{PLH}	4.5		1	18	30		38	ns
$A,B \rightarrow Y (L \rightarrow H)$		6.0				26		33	
D		2.0				150		190	
Propagation time	t PHL	4.5			17	30		38	ns
$A, B \rightarrow Y (H \rightarrow L)$		6.0				26		33	
D		2.0				175		220	
Propagation time	t PLH	4.5			19	35		44	ns
$C \rightarrow Y (L \rightarrow H)$		6.0		1		30		37	
D		2.0				150		190	
Propagation time	t PHL	4.5		}	18	30	}	38	ns
$C \rightarrow Y (H \rightarrow L)$		6.0		}		26	}	33	
		2.0				125		155	
3-state propagation time	t PHZ	4.5	$R_L=1k\Omega$	1	15	25		31	ns
$(H \rightarrow Z)$		6.0				21		26	
		2.0				125		155	
3-state propagation time	t PLZ	4.5	$R_L=1k\Omega$		15	25		31	ns
(L→Z)		6.0				21		26	
		2.0				100		125	
3-state propagation time	t _{PZH}	4.5	$R_L=1k\Omega$		11	20		25	ns
(Z→H)		6.0				17		21	
		2.0				175		220	
3-state propagation time	t PZL	4.5	$R_L=1k\Omega$		19	35	}	44	ns
(Z→L)		6.0				30		37	



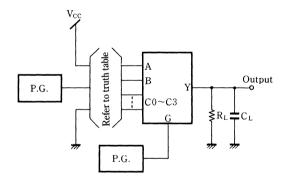
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}
 - 1 Measuring Circuit



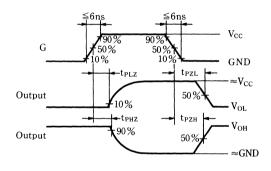


(2) t_{PHZ}, t_{PZH}

1. Measuring Circuit

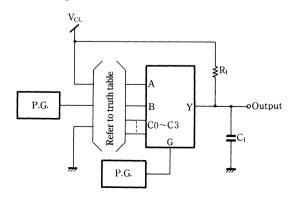


2. Waveforms



(3) t_{PLZ} , t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.



MN74HC365/MN74HC365S

Hex TRI-STATE Buffers

■ Description

MN74HC365/MN74HC365S are high-speed non-inverted buffers consisting of six tri-state outputs. Large current output makes possible high-speed operation for driving a large capacity bus line. The hex gate can be simultaneously controlled by two tri-state control inputs $(\overline{G}_1 \text{ and } \overline{G}_2)$ when output becomes enabled at LOW level.

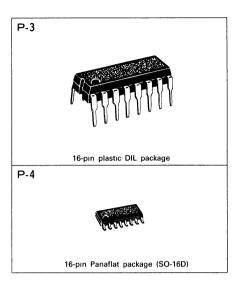
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

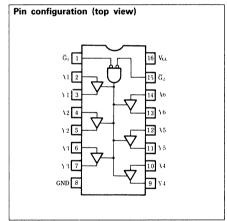


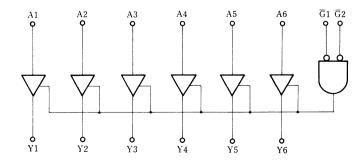
	Input		Output
<u>G</u> 1	G2	A	Y
Н	×	×	Hı-Z
×	Н	×	Hı-Z
L	L	Н	Н
L	L	L	L

Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance







	Paramete	er	Symbol	Rating	Unit	
Supply volta	oltage		$V_{\rm cc}$	-0.5∼+7.0	V	
Input/output	voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V	
Input protec	tion diode current		I _{IK}	±20	mA	
Output paras	sitic diode current		Іок	±20	mA	
Output curre	ent		Io	±35	mA	
Supply curre	ent		Icc, Ignd	±70	mA	
Storage tem	emperature range		Tstg	-65~+150	$^{\circ}$	
	MNIZALICOGE	Ta=-40~+60℃	Po	400	m W	
Power			F))	Decrease to 200mW at the rate of 8mW/°C	III VV	
dissipation	MN74HC365S	Ta=-40~+60℃	D	275	mW	
	WIN74IIC3035	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m vv	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	$V_{\rm I}, V_{\rm O}$		0~Vcc	V
Operating temperature range	TA		−40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr,tf	4.5	0~500	ns
		6.0	0~400	ns

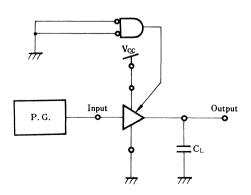
			Tes	st Conditio	ons		Te	mperati	ıre		
Parameter	Symbol	V _{CC}	Vı	Io		•	Γa = 25 °	С	Ta=-40)~+85℃	Unit
		(•)	•	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15		İ	3.15		V
		6.0				4.2			4.2		
Input LOW voltage		2.0						0.3		0.3	
	V _{II} .	4.5						0.9		0.9	V
		6.0						1.2		1.2	
Output HIGH voltage		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	Vih	-20.0	μA	4.4	4.5		4.4		
	V_{OH}	6.0	or	-20.0	μA	5.9	6.0	İ	5.9		V
		4.5	V_{fL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	VoL	6.0	or	20.0	μA		0.0	0.1	ļ	0.1	V
		4.5	VIL	6.0	mA			0.32	Ì	0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	,		V _I =V _{IH} or V _{IL} V ₀ =V _{CC} or GND				105		1.5.0		
current	Ioz	6.0					±0.5		±5.0	μA	
Quiescent supply current	Icc	6.0	$V_I = V_C$	cc or GNI	D, I ₀ =0			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C

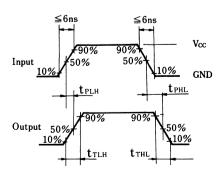
					Te	mperati	ıre		
Parameter	Symbol	V _{CC} (V)	Test Conditions	,	Ta=25°	2	Ta=-40)~+85℃	Unit
		_ ` ' '		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5		1	7	15		19	ns
		6.0		1		13		16	
Output fall time		2.0				75		95	
	t _{THL}	4.5			6	15	1	19	ns
		6.0				13		16	
Propagation time (L→H)		2.0				75		95	
	tplh	4.5			8	15		19	ns
		6.0		1	1	13		16	
		2.0				75		95	
Propagation time	t PHL	4.5			7	15		19	ns
(H→L)		6.0				13		16	
3-state propagation time		2.0				100		125	
	t PHZ	4.5	$R_L = 1 k\Omega$		12	20		25	ns
(H→Z)		6.0				17		21	
2 atata		2.0				125		155	
3-state propagation time	t PLZ	4.5	$R_L = 1 k\Omega$		16	25		31	ns
(L→Z)		6.0				21		26	
2 -4 -4		2.0				100		125	
3-state propagation time	t _{PZH}	4.5	$R_L = 1 k\Omega$		11	20		25	ns
(Z→ H)		6.0				17		21	
2 -4-4		2.0				100		125	
3-state propagation time	t PZL	4.5	$R_L = 1 k\Omega$		13	20		25	ns
(Z→L)		6.0				17		21	

• Switching Time Measuring Circuit and Waveforms

- (1) t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

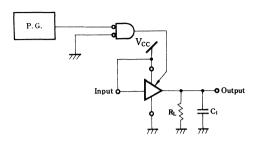


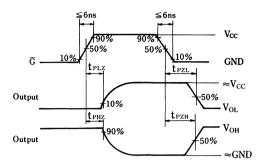
2. Waveforms



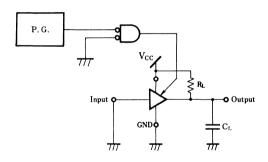


- (2) t_{PHZ}, t_{PZH}
 - 1. Measuring Circuit





- $\left(3\right)\,t_{PLZ}\!/t_{PZL}$
 - 1 1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC366/MN74HC366S

Inverting Hex TRI-STATE Buffers

■ Description

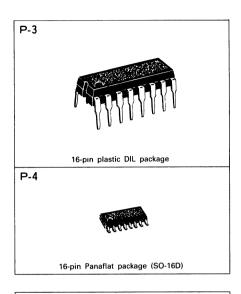
MN74HC366/MN74HC366S are high-speed inverting buffers consisting of six tri-state outputs. Large current output makes possible high-speed operation for driving a large capacity bus line. Six gates can be simultaneously controlled by two tri-state control inputs $(\overline{G}_1$ and $\overline{G}_2)$ where output becomes enable at LOW. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and family as standard 54LS/74LS logic family.

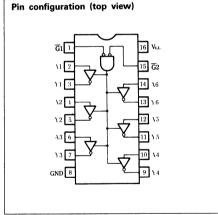
■ Truth Table

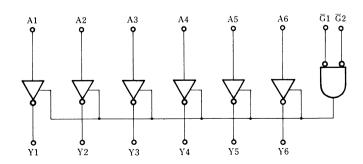
Output $\overline{G}1$ \overline{G} 2 Y Α Н × X Hi-Z × Н × Hı-Z L L L Н L L L Н

Note:

- 1. X: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance







	Paramete	r	Symbol	Rating	Unit					
Supply volta	ge		$V_{\rm cc}$	−0.5~+7.0	V					
Input/output	voltage		V_1, V_0	$-0.5 \sim V_{\rm CC} + 0.5$	V					
Input protection diode current			I_{lK}	±20	mA					
Output parasitic diode current			Іок	±20	mA					
Output current			Io	±35	mA					
Supply curre	Supply current			rent		rent		Icc, Ignd	± 70	mA
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$					
	MN74HC366	Ta=-40~+60 ℃	P_{D}	400	W					
Power	M117411C300	Ta=+60~+85 °C	F))	Decrease to 200mW at the rate of 8mW/°C	m W					
dissipation	MN74HC366S	Ta=-40~+60°C	ъ	275	117					
	WIN 411C3003	Ta=+60~+85 ℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m W					

■ Operating Conditions

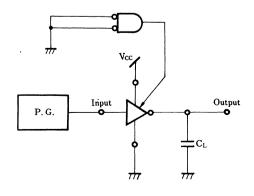
Parameter	Symbol	Vcc(V)	Rating	Unit	
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V	
Input/output voltage	V_{I},V_{O}		0~Vcc	V	
Operating temperature range	TA		-40~+ 85	°C	
Input rise and fall time		2.0	0~1000	ns	
	t _r ,t _f	4.5	0~500	ns	
		6,0	0~400	ns	

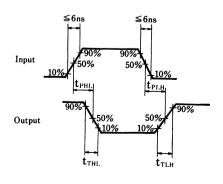
			Te	st Conditi	ons		Te	mperati	ıre		
Parameter	Symbol	V _{CC} (V)	Vı	Io		•	Γa=25°	2	Ta=-40	0~+85℃	Unit
		(•)	٧,	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
Input LOW voltage		2.0						0.3		0.3	
	VIL	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
•		4.5	V_{1L}	-6.0	mA	3.86		1	3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Ιι	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	Ioz	6.0	V _I =V _{IH} or V _{IL} V _O =V _{CC} or GND				+0 5		±5.0		
current	10Z	0.0					±0.5		_ ±5.0	μΑ	
Quiescent supply current	Icc	6.0	$V_I = V_C$	cc or GNI	$I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

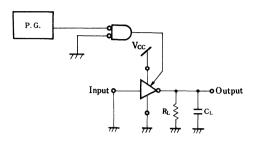
					Te	mperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Γa=25 °	2	Ta=-40)~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t TLH	4.5			7	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15]	19	ns
		6.0				13		16	
Propagation time		2.0				75		95	
	t PLH	4.5		ļ	9	15		19	ns
(L→H)		6.0				13	Ì	16	
Propagation time		2.0				75		95	
(H→L)	t PHL	4.5			8	15		19	ns
(n→L)		6.0		1		13		16	
Propagation time		2.0				100		125	
(H→Z)	t PHZ	4.5	$R_L = 1 k\Omega$		13	20	İ	25	ns
(H→Z)		6.0		ł		17		21	
3-state propagation time		2.0				150		190	
	t _{PLZ}	4.5	$R_L = 1 k\Omega$		18	30		38	ns
(L→Z)		6.0				26		33	
3-state propagation time		2.0				100		125	
	t _{PZH}	4.5	$R_L = 1 k\Omega$		11	20		25	ns
(Z→H)		6.0				17		21	
3-state propagation time		2.0				100		125	
	t _{PZL}	4.5	$R_L = 1 k\Omega$		13	20		25	ns
(Z→L)		6.0				17		21	

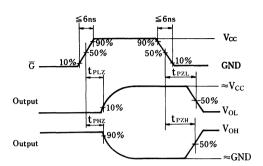
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , t_{PLH} , t_{PHL}
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})



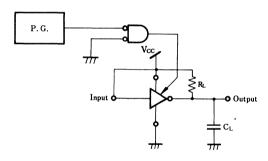


- (2) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit





- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC367/MN74HC367S

Hex TRI-STATE Buffers

■ Description

MN74HC367/MN74HC367S are high-speed non-inverted buffers consisting of six tri-state outputs. Large current output makes possible high-speed operation for driving a large bus line. Two inputs $(\overline{G}_1$ and $\overline{G}_2)$ are available where output becomes enable at LOW, and \overline{G}_1 controls four gates and \overline{G}_2 controls two gates respectively.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

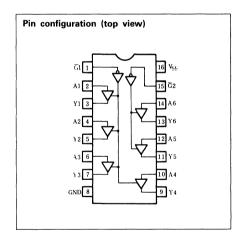
P-3 16-pin plastic DIL package P-4 16-pin Panaflat package (SO-16D)

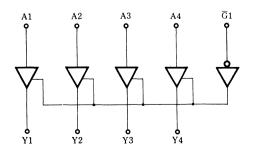
■ Truth Table

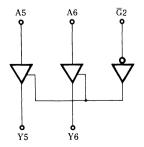
Inp	out	Output
G	A	Y
Н	×	Hı-Z
L	Н	Н
L	L	L

Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance









	Paramete	er	Symbol	Rating	Unit
Supply voltage	ge		V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protection diode current			I _{IK}	±20	mA
Output parasitic diode current			Іок	±20	mA
Output curre	Output current			±35	mA
Supply curre	Supply current			±70	mA
Storage tem	perature range	rature range		-65~+150	°C
	MNIZALICOCZ	Ta=-40~+60°C	P_{D}	400	mW
Power	MN74HC367	Ta=+60~+85℃	Г))	Decrease to 200mW at the rate of 8mW/°C	m w
dissipation	MN74HC367S	Ta=-40~+60℃	D.	275	117
	MIN/4HC30/5	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m W

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	TA		-40~+8 5	°C
Input rise and fall time		2.0	0~1000	ns
	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

		,,	Те	st Conditi	ons		Te	emperat	ure		
Parameter	Symbol	(V)	Vı	Io		,	Γa=25 °	С	Ta=-40)~+85℃	Unit
		, , ,		-(/	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5]		3.15			3.15		V
		6.0				4.2			4.2		
Input LOW voltage		2.0						0.3		0.3	
	VII.	4.5						0.9	1	0.9	V
		6.0						1.2	İ	1.2	
Output HIGH voltage		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
	Vон	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{fL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μΑ		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μ A		0.0	0.1	1	0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_1	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	Ioz	6.0	$V_I = V$	THOR VI	I.			40.5		+50	
current	10Z	0.0	Vo=Vcc or GND				± 0.5		±5.0	μΑ	
Quiescent supply current	$I_{\rm cc}$	6.0	$V_I = V_C$.c or GNI	$I_0 = 0$			8.0		80.0	μA

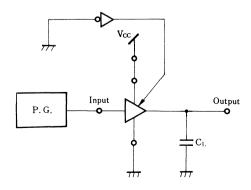
■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

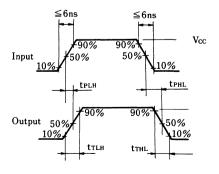
		V _{CC} (V)	Test Conditions	Temperature					
Parameter	Symbol			Ta=25 ℃		Ta=-40~+85℃		Unit	
				min.	typ.	max.	min.	max.	į
Output rise time	t _{TLH}	2.0				75		95	
		4.5			7	15		19	ns
		6.0				13		16	
Output fall time	t _{THL}	2.0				75		95	
		4.5			6	15	ļ	19	ns
		6.0				13		16	
Propagation time $(L \rightarrow H)$	t _{PLH}	2.0				75		95	
		4.5			7	15		19	ns
		6.0				13		16	
Propagation time $(H \rightarrow L)$	t _{PHL}	2.0				75		95	
		4.5			6	15		19	ns
		6.0				13	1	16	
3-state propagation time	t _{PHZ}	2.0				100		125	
		4.5	$R_L = 1 k\Omega$		12	20		25	ns
		6.0				17	İ	17	
3-state propagation time	t _{PLZ}	2.0				100		125	
		4.5	$R_L = 1 k\Omega$		13	20	ĺ	25	ns
		6.0				17		17	
3-state propagation time	t _{PZH}	2.0				75		95	
		4.5	$R_L = 1 k\Omega$		9	15		19	ns
		6.0				13		16	
3-state propagation time	t _{PZL}	2.0				75		95	
		4.5	$R_L = 1 k\Omega$		10	15		19	ns
		6.0				13		16	

• Switching Time Measuring Circuit and Waveforms

- (1) t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}
 - 1. Measuring Circuit

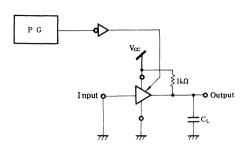
2. Waveforms



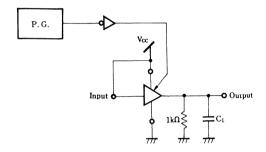


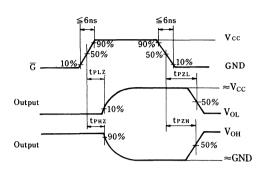


- (2) t_{PHZ}, t_{PZH}
 - 1. Measuring Circuit



- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit





2. Waveforms

See above [2] 2. for waveforms.

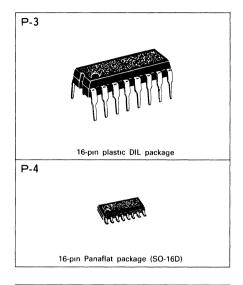
MN74HC368/MN74HC368S

Inverting Hex TRI-STATE Buffers

■ Description

MN74HC368/MN74HC368S are high-speed inverting buffers consisting of six tri-state outputs. Large current output makes possible high-speed operating for driving a large capacitance bus line. Two inputs $(\overline{G}_1 \text{ and } \overline{G}_2)$ are available where output becomes enable at LOW, and \overline{G}_1 controls four gates and \overline{G}_2 controls two gates respectively.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

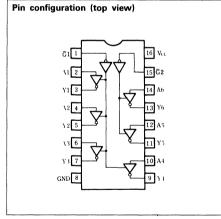


■ Truth Table

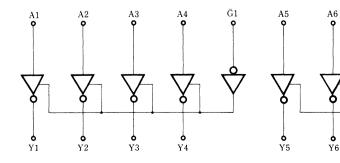
In	Output		
\overline{G}	A	Y	
Н	×	Hi-Z	
L	Н	L	
L	L	Н	

Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance



 $\overline{G}2$





	Parameter		Symbol	Rating	Unit	
Supply voltag	ge		V_{CC}	−0.5~+7.0	V	
Input/output voltage			V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V	
Input protection diode current			I _{IK}	±20	mA	
Output parasitic diode current			Іок	±20	mA	
Output current			Io	±35	mA	
Supply curre	nt		Icc, IGND	±70	mA	
Storage temp	perature range		Tstg	-65~+150	°C	
	MNGALIGOGO	Ta=-40~+60°C	ъ	400	m W	
Power dissipation	MN74HC368	Ta=+60~+85℃	P_0	Decrease to 200mW at the rate of 8mW/°C	m vv	
	MN74UC2606	Ta=-40~+60℃	ъ	275	117	
	MN74HC368S	Ta=+60~+85 ℃	P _D	Decrease to 200mW at the rate of 3.8mW/°C	m W	

■ Operating Conditions

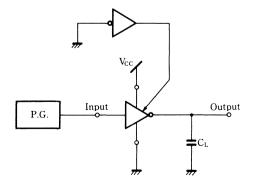
Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

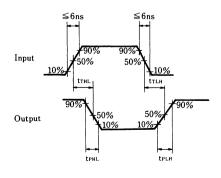
		17	Test Conditions			Te	mperati	ıre			
Parameter	Symbol	V _{CC} (V)	Vi	Io		,	Ta=25°	C	Ta=-40)~+85°C	Unit
				10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{II}	4.5						0.9	1	0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
		4.5	ViH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{II}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	Ioz	6.0	$V_1 = V$	TH or V	II.			±0.5		±5.0	μΑ
current		0.0	Vo=V	lu or (GND					-3.0	<i>μ</i> Λ
Quiescent supply current	$I_{\rm CC}$	6.0	$V_I = V_C$	c or GNI	$I_0=0$			8.0		80.0	μA

■ AC	Characteristics	(GND=0V,	Input	transition	time	≦6ns,	$C_i = 50 pF$	1
------	-----------------	----------	-------	------------	------	-------	---------------	---

					Temperature					
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25 °	2	Ta=-40)~+85℃	Unit	
		L (*/		min.	typ.	max.	min.	max.		
		2.0				75		95		
Output rise time	t _{TLH}	4.5			7	15		19	ns	
		6.0				13		16		
		2.0				75		95		
Output fall time	t _{THL}	4.5			6	15		19	ns	
		6.0		}		13		16		
Propagation time (L→H)		2.0				75		95		
	t _{PLH}	4.5			7	15		19	ns	
		6.0				13		16		
Propagation time		2.0				75		95		
(H→L)	t PHL	4.5			6	15		19	ns	
(H→L)		6.0				13		16		
		2.0				125		155		
3-state propagation time	t _{PHZ}	4.5	$R_L = 1 k\Omega$		13	25		31	ns	
		6.0				21		26		
		2.0				125		155		
3-state propagation time	t PLZ	4.5	$R_L = 1 k\Omega$		12	25		31	ns	
		6.0				21		26		
		2.0				100		125		
3-state propagation time	t _{PZH}	4.5	$R_L = 1 k\Omega$		9	20		25	ns	
		6.0				17		21		
		2.0				100	,	125		
3-state propagation time	t _{PZL}	4.5	$R_L = 1 k\Omega$		10	20		25	ns	
		6.0				17		21		

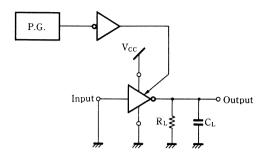
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , t_{PLH} , t_{PHL}
 - 1. Measuring Circuit

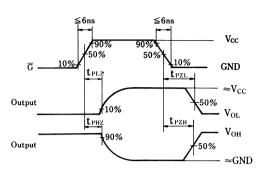




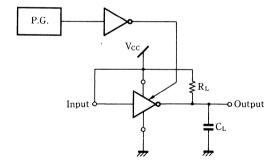


- [2] t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit





- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

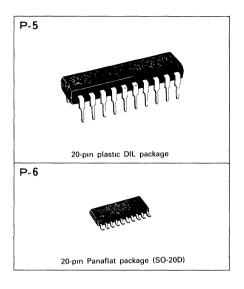
MN74HC373/MN74HC373S

Octal TRI-STATE D-Type Latches

■ Description

MN74HC373/MN74HC373S contain octal tri-state D-type latches. High output driving capacity and tri-state outputs are suited for the use of a common bus line in the bus utilized system. When output disable input is "L" and latch enable input is "H", the output outputs the data input. When latch enable is "L", data input is maintained as is until when latch enable input becomes "H" again. Output disable input is "H", all inputs become high impedance state, regardless of other inputs and data-hold circuit.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

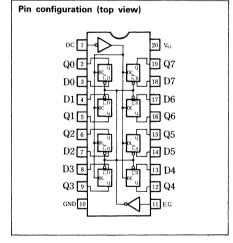


■ Truth Table

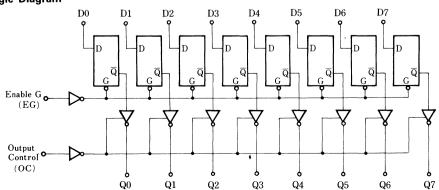
Output Control	Enable G	D	Output		
L	Н	Н	Н		
L	Н	L	L		
L	L	×	Q_0		
Н	×	×	Hi-Z		

Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. H₁-Z: High impedance
- 3. Q_O: Q level prior to determination of input condition shown in table



■ Logic Diagram



	Paramete	er	Symbol	Rating	Unit
Supply voltag	ge			−0.5~+7.0	V
Input/output	Input/output voltage			$-0.5 \sim V_{CC} + 0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			Iok	± 20	mA
Output curre	Output current			± 35	mA
Supply curre	nt		Icc, IGND	±70	mA
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$
	MN74HC373	Ta=-40~+60℃	P_{D}	400	11/
Power	MIN74IIC373	Ta=+60~+85 ℃	[F])	Decrease to 200mW at the rate of 8mW/°C	m W
dissipation	MN74HC373S	$Ta = -40 \sim +60 \text{°C}$	D.	275	. W
	MIN74HC3735	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	m W

■ Operating Conditions

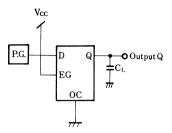
Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	TA		-40~+8 5	°C
		2.0	0~1000	ns
Input rise and fall time	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

,		37			Test Conditions		Temperature				
Parameter	Symbol	V _{CC} (V)	Vı	Io		,	Γa=25°		Ta=-40)~+85℃	Unit
			• •	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	Von	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	V _{IL}	- 6.0	mA	3.86			3.76		
		6.0		- 7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	Vih	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V _{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I ₁	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	T	6.0	$V_I = V$	THOR V	11.			105		15.0	
current	Ioz	0.0	Vo=Vcc or GND				± 0.5		±5.0	μA	
Quiescent supply current	I_{CC}	6.0	$V_1 = V_0$	c or GNI), I ₀ =0			8.0		80.0	μA

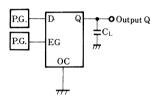
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

					Te	mperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions	,	Ta=25 °	2	Ta=-40)~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			7	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				125		155	
D→Q (L→H)	t _{PIH}	4.5			15	25		31	ns
2 (11)		6.0				21		26	
Propagation time		2.0		1		125		155	
D→Q (H→L)	t PHL	4.5			14	25		31	ns
D •Q (II •E)		6.0				21		26	
Propagation time		2.0				175		220	
Enable $G \rightarrow Q(L \rightarrow H)$	t _{PIH}	4.5			19	35		44	ns
Enable G -Q(L-II)		6.0				30		37	
Propagation time		2.0				125		155	
Enable $G \rightarrow Q(H \rightarrow L)$	t PHL	4.5			15	25		31	ns
Enable 0 -Q(II-L)		6.0				21		26	
3-state propagation time		2.0				150		190	
(H→Z)	t PHZ	4.5	$R_L = 1 k\Omega$		17	30		38	ns
(II · Z)		6.0				26		33	
3-state propagation time		2.0				150		190	
(L→Z)	t PI 7	4.5	$R_L = 1 k\Omega$		18	30		38	ns
(E · E)		6.0				26		33	
3-state propagation time		2.0				125		155	
(Z→H)	t _{P7H}	4.5	$R_L = 1 k\Omega$		14	25		31	ns
(Z · II)		6.0				21		26	
3-state propagation time		2.0				125		155	
(Z→L)	t _{PZL}	4.5	$R_L = 1 k\Omega$		15	25		31	ns
(Z · L)		6.0				21		26	
		2.0				100		125	
Minimum Set-up time	t _{su}	4.5			2	20		25	ns
		6.0				17		21	
		2.0			_	0		0	
Mınimum Hold time	th	4.5				0		0	ns
		6.0				0		0	

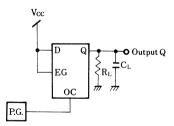
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , $t_{PLH}/t_{PHL}(D\rightarrow Q)$
 - 1. Measuring Circuit



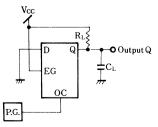
- (2) $t_{PLH}/t_{PHL}(ENG \rightarrow Q)$, t_{su} , t_h
 - 1. Measuring Circuit

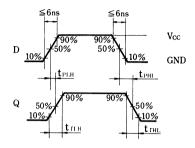


- (3) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit

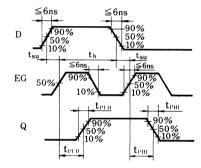


- (4) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit

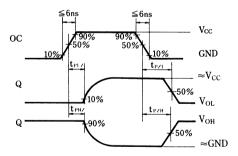




2. Waveforms



2. Waveforms



2. Waveforms

See above [3] 2. for waveforms.

MN74HC374/MN74HC374S

Octal TRI-STATE D-Type Flip-Flops

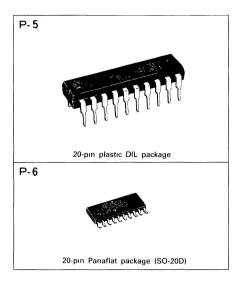
■ Description

MN74HC374/MN74HC374S contain eight high speed D-type flip-flops with tri-state outputs.

High output driving capability and tri-state outputs are suited for the use of a common bus line in the bus utilized system.

D input data satisfying set-up time is transferred to the output on the positive-going edge of clock input. When output disable input is HIGH, all outputs become high impedance state regardless of other input data and the data-hold circuit.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

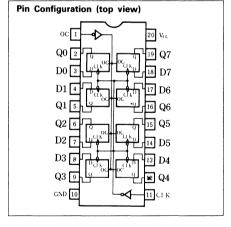


■ Truth Table

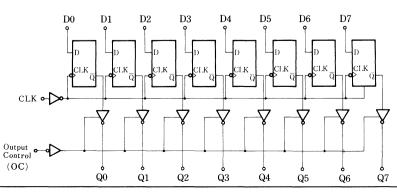
	Input		Output
Output Control	CLK	D	Q
L		Н	Н
L	5	L	L
L	L	×	Q_{0}
Н	×	×	Hi-Z

Note:

- 1. : Data input is transferred to output on the positive-going edge from LOW to HIGH
- 2. ×: Either HIGH or LOW; it doesn't matter
- 3. Q_0 : Q level prior to determination of input condition shown in table
- 4. Hi-Z High impedance



■ Logic Diagram (1 gate)



	Paramete	r	Symbol	Rating	Unit									
Supply voltage	tage		ge		age		age		Vcc	-0.5~+7.0	V			
Input/output	Input/output voltage			output voltage		utput voltage		tput voltage		put voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	Input protection diode current			±20	mA									
Output paras	Output parasitic diode current			±20	mA									
Output curre	Output current			±35	mA									
Supply curre	ent		Icc, IGND	±70	mA									
Storage tem	perature range		Tstg	$-65 \sim +150$	$^{\circ}$									
	MN74HC374	Ta=-40~+60 ℃	P_{D}	400	m W									
Power	MN74HC374	Ta=+60~+85 °C	P))	Decrease to 200mW at the rate of 8mW/°C	m vv									
dissipation	MN74HC374S	Ta=-40~+60 ℃	ъ	275	m W									
	MIN/4/1C3/45	Ta=+60~+85 °C	Po	Decrease to 200mW at the rate of 3.8mW/°C	m vv									

■ Operating Conditions

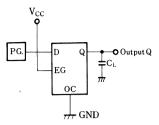
Item	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V ₁ , V ₀		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
•		6.0	0~400	ns

		17	Те	st Conditi	ons		Te	mperati	ure		
Parameter	Symbol	V _{CC} (V)	Vı	Io		,	Γa=25 °	2	Ta=-40)~+85℃	Unit
		(- /	*1	10	Unit	mın.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4	1	
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V _{II} .	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μΑ		0.0	0.1		0.1	
		4.5	ViH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	Vil	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	II	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state		6.0	V _I =V _{IH} or V _{II}				105		150		
current	Ioz	6.0	V _o =V	$V_O = V_{CC}$ or GND				± 0.5		±5.0	μ A
Quiescent supply current	I_{cc}	6.0	$V_I = V_C$	c or GNI), I ₀ =0			8.0		80.0	μA

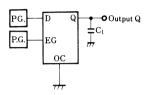
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

		37			Tei	nperatu	re		
Parameter	Symbol	Vcc (V)	Test Conditions	•	Ta = 25°	2	Ta=-40	~+85℃	Unit
		,		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75	l	95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				150		190	
CLK→Q (L→H)	t PLH	4.5			18	30		38	ns
CLK-Q (L-II)		6.0				26		33	
Propagation time		2.0				150		190	
CLK→Q (H→L)	t PHL	4.5			19	30		38	ns
CLK-Q (II-L)		6.0				26		33	
3-state propagation time		2.0				150		190	
(H→Z)	t _{PHZ}	4.5	$R_L = 1 k\Omega$		18	30		38	ns
(II→Z)		6.0				26		33	
3-state propagation time		2.0				150		190	
(L→Z)	t PLZ	4.5	$R_L = 1 k\Omega$		18	30		38	ns
(L · L)		6.0				26		33	
3-state propagation time		2.0				100		125	
(Z→H)	t _{PZH}	4.5	$R_L = 1 k\Omega$		13	20		25	ns
(Z · II)		6.0				17		21	
3-state propagation time		2.0				125		155	
(Z→L)	t PZL	4.5	$R_L = 1 k\Omega$		15	25		31	ns
(E · E)		6.0				21		26	
		2.0				75		95	
Mınımum pulse wıdth	tsu	4.5			2	15		19	ns
		6.0				13		16	
		2.0			_	0		0	
Mınımum Hold time	th	4.5			_	0		0	ns
		6.0				0		0	
		2.0		6			4		
Maximum clock frequency	fmax	4.5		30	64		24		MHz
		6.0		35			28		

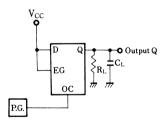
- Switching Time Measuring Circuit and Waveforms
- [1] t_{1LH} , t_{THL} , $t_{PLH}/t_{PHL}(D \rightarrow Q)$
 - 1. Measuring Circuit



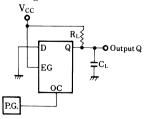
- (2) $t_{PLH}/t_{PHL}(ENG \rightarrow Q)$
 - 1. Measuring Circuit

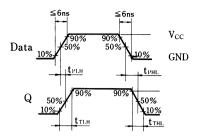


- (3) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit

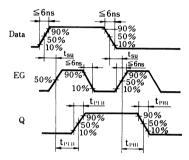


- (4) t_{PLZ}, t_{PZL}
 - 1. Measuring Circuit

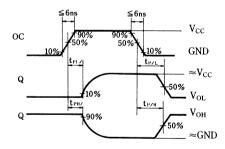




2. Waveforms



2. Waveforms (tphz, tpzh, tplz, tpzl)



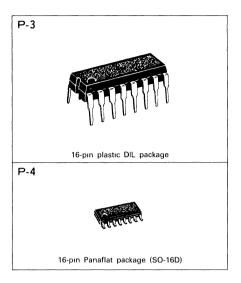
MN74HC375/MN74HC375S

4-Bit Bistable Latches

■ Description

MN74HC375/MH74HC375S are bistable latches with four bit Q, \overline{Q} output. These are suited for temporary binary data memory circuits between the data processing unit and the I/O, or between display units. Data at data input (D) are transferred to output Q when enable pin (G) is "H"; output Q follows the data input state so long as the enable is "H". When enable becomes "L", output Q is maintained as is until when the enable becomes "H". Output Q indicates the data input state when the enable changes from "H" to "L".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



■ Truth Table

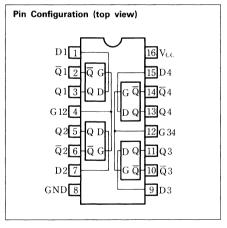
In	put	Output				
D	G	Q	$\overline{\mathbb{Q}}$			
L	Н	L	Н			
Н	Н	Н	L			
×	L	Q_0	$\overline{\overline{\mathbf{Q}}}_{0}$			

Note: 1. ×:

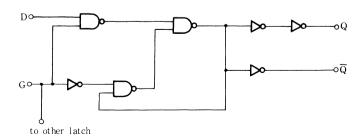
Either HIGH or LOW; it doesn't matter

2. Q_O : Q level prior to determination of input condition shown in table

3. \overline{Q}_{O} Q level prior to determination of input condition shown in



■ Logic Diagram





	Paramete	r	Symbol	Rating	Unit
Supply voltage	Supply voltage			$-0.5\sim+7.0$	V
Input/output	Input/output voltage			$-0.5 \sim V_{CC} + 0.5$	V
Input protec	Input protection diode current			±20	mA
Output paras	Output parasitic diode current			± 20	mA
Output current			Io	±25	mA
Supply curre	ent		Icc, IGND	±50	mA
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$
	MNGALLCOGE	Ta=-40~+60°C	P_{D}	400	m W
Power	MN74HC375	Ta=+60~+85°C	[FD	Decrease to 200mW at the rate of 8mW/°C	m vv
dissipation		Ta=-40~+60°C	D	275	m W
	MN74HC375S	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m vv

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V ₁ ,V ₀		0∼Vcc	V
Operating temperature range	TA		-40~+85	°C
Input rise and fall time		2.0	0~1000	ns
	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

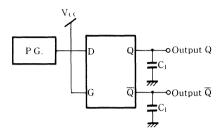
		W	Tes	st Conditio	ons		Te	mperatu	ıre		
Parameter	Symbol	Vcc (V)	3.7	T		Ta=25 ℃			Ta=-40~+85°C		Unit
		. (•)	V ₁ I ₀	Unit	mın.	typ.	max.	mın.	max.		
Input HIGH voltage		2.0				1.5			1.5		
	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	Vон	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V _{II}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_{I} = V$	cc or G	ND			±0.1		±1.0	μΑ
Quiescent supply current	Icc	6.0	$V_{I} = V_{C}$	c or GNI	$D, I_0=0$			8.0		80.0	μA

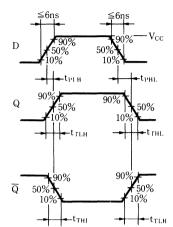
AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

	T				T	emperat	ure		
Parameter	Symbol	V _{CC}	Test Conditions		Ta=25 °	2	Ta=-40)~+85℃	Unit
		`*′		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t TLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15		19	ns
		6.0		1		13		16	
Propagation time		2.0				100		125	
	t PLH	4.5			10	20		25	ns
D→Q (L→H)		6.0				17		21	
Propagation time		2.0				100		125	
D \rightarrow Q (H \rightarrow L)	t _{PHL}	4.5			11	20		25	ns
D-Q (II-L)		6.0				17		21	
Propagation time		2.0				100		125	
$D \rightarrow \overline{Q} (L \rightarrow H)$	t PLH	4.5			11	20		25	ns
D-Q (L-n)		6.0				17		21	
Propagation time		2.0				100		125	
$D \rightarrow \overline{Q} (H \rightarrow L)$	t _{PHL}	4.5			9	20		25	ns
D-Q (n-L)		6.0				17		21	
Propagation time		2.0				125		155	
$G \rightarrow Q (L \rightarrow H)$	t PLH	4.5			12	25		31	ns
G *Q (E *II)		6.0				21		26	
Propagation time		2.0				125	1	155	
G→Q (H→L)	t PHL	4.5			14	25		31	ns
GQ (II -L)		6.0				21		26	
Propagation time		2.0				125		155	
$G \rightarrow \overline{Q} (L \rightarrow H)$	t PLH	4.5			14	25		31	ns
G • Q (E • H)		6.0				21		26	
Propagation time		2.0				125		155	
$G \rightarrow \overline{Q} (H \rightarrow L)$	t PHL	4.5			10	25		31	ns
		6.0				21		26	
		2.0		}		100		125	
Mınımum Set-up time	t _{su}	4.5			2	20		25	ns
		6.0				17		21	
		2.0			_	0		0	
Mınımum Hold time	th	4.5			-	0		0	ns
		6.0				0		0	
		2.0				125		155	
Mınımum pulse width	t _w	4.5			1	25		31	ns
		6.0				21		26	

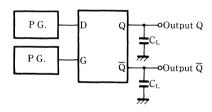


- Switching Time Measuring Circuit and Waveforms
- (1) $t_{TLH}, t_{THL}, t_{PLH}/t_{PHL}(D \rightarrow Q, \bar{Q})$
 - 1. Measuring Circuit

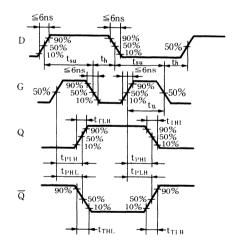




- (2) $t_{PLH}/t_{PHL}(G\rightarrow Q, \bar{Q})$, t_{W} , t_{SU} , t_{h}
 - 1. Measuring Circuit



2. Waveforms



MN74HC377/MN74HC377S

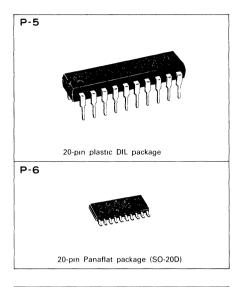
Octal D-Type Flip-Flop with Enable Data

■ Description

MN74HC377/377S contain eight high-speed D-type flip-flops with enable data.

D input data satisfying set-up time is transferred to the output Q on the rising edge of clock input, when enable data input $\overline{\text{CE}}$ is "L". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



Pin Configuration (top view)

C E II Q0 [2 D0 [3 D1 [4 Q1 [5 Q2 [6

D2 7

D3 [8

Q4 [9

GND TO

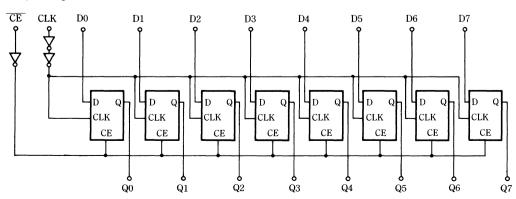
■ Truth Table

On austral a Mada		Input		Output
Operating Mode	CLK	CE	Dn	Qn
Load "1"	5	L	Н	Н
Load "0"	5	L	L	L
Hold (Do nothing)	5	Н	×	No Change
	Н	Н	×	No Change

Note:

- 2. ×: Either HIGH or LOW; it doesn't matter.

■ Logic Diagram





20 V_{CC}

151 Q5

13 D4

III CLK

	Paramet	er	Symbol	Rating	Unit
Supply voltage				-0.5~+7.0	V
Input/output voltage			V _I , V _O	-0.5~V _{CC} +0.5	V
Input protect	ion diode current		I_{IK}	±20	mA
Output paras	Output parasitic diode current			±20	mA
Output current		I_{O}	±25	mA	
Supply curren	Supply current		I _{CC} , I _{GND}	±50	mA
Storage temp	oerature range		Tstg	-65~+150	°C
	MN74HC377	Ta=-40~+60°C	P_{D}	400	mW
Power	WIN74HC377	Ta=+60~+85°C	I D	Decrease to 200mW at the rate of 8mW/°C	11177
dissipation MN74HC377S		Ta=-40~+60°C	P_{D}	275	mW
	WINT-HICST'IS	Ta=+60~+85°C	I.D	Decrease to 200mW at the rate of 3.8mW/°C	111 44

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0∼V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
Input rise and fall time		V _{CC} =2.0V	0~1000	ns
	t _r , t _f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0V	0~400	ns

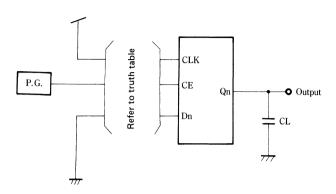
			Test Conditions				T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vi	Io			Ta=25°C		Ta=-40	~+85°C	Unit
		(,)	V I	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	V
		2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.5		V
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		V
		6.0		-5.2	mA	5.36			5.26		V
		2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	V
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V _{IL}	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I _I	6.0	V _I =	V _{CC} or G	ND			±0.1		±0.1	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CC}$	or GND	, $I_O=0$			8.0		80.0	μA

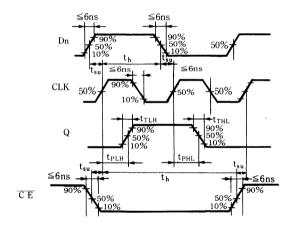
■ AC Characteristics (GND=0V, Input transistion tiem \leq 6ns, C_L =50pF)

					T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta=-40	~+85°C	Unit
		\.''		mın.	typ.	max.	mın.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5		1		15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time t	t_{THL}	4.5				15		19	ns
		6.0				13		16	
Propagation time		2.0				150		190	
CLK→D	t _{PLH}	4.5				30		38	ns
(L→H)		6.0	- Turn			26		33	
Propagation time CLK→D (H→L)		2.0				150		190	
	t _{PHL}	4.5				30		38	ns
		6.0				26		33	
Mınımum		2.0				100		125	
Set-up time	t _{su}	4.5				20		25	ns
D		6.0				17		21	
Mınimum		2.0				100		125	
Set-up time	t _{su}	4.5				20		25	ns
CE		6.0			ļ	17		21	
M: II-14		2.0				0		0	
Minimum Hold time D	t _h	4.5				0		0	ns
		6.0				0		0	
Mınımum Hold tıme		2.0				0	1	0	
CE	t _h	4.5				0		0	ns
		6.0				0		0	
M		2.0				100		125	
Mınımum pulse width CLK	t _w	4.5				20		25	ns
CLIX		6.0				17		21	
3.5		2.0		6			4		
Maximum clock frequency	f_{max}	4.5		30			24		MHz
requericy		60		35			28		



- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})





MN74HCT377/MN74HCT377S

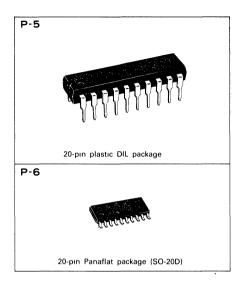
Octal D-Type Flip-Flop with Enable Data (TTL Input)

■ Description

MN74HCT377/MN74HCT377S contain eight high-speed D-type flip-flops with enable data. D input data satisfying set-up time is transferred to the output Q on the positive-going edge of clock input, when enable data input \overline{CE} is "L".

All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2V or more is logic "1". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



Pin Configuration (top view)

CEL

D0 🖪

D1 4

Q1 5

Q2 [6

D2 7

D3 🛭

Q3 [9

GND TO

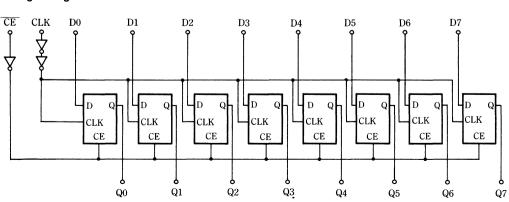
■ Truth Table

Operating Mode		Input		Output		
Operating Mode	CLK	CE	Dn	Qn		
Load "1"		L	Н	Н		
Load "0"	5	L	L	L		
Hold (Do nothing)	5	Н	×	No Change		
noid (Do nothing)	Н	Н	×	No Change		

Note:

- 1. _____: Data input is transferred to output on the positive-going edge from LOW to HIGH.
- 2. ×: Either HIGH or LOW; it doesn't matter.

`■ Logic Diagram





201 V_{cc} 191 Q7

181 D7

71 D6

6 Q6

151 Q5

T41 D5

3 D4

[2] Q4

III CLK

	Parameter			Rating	Unit								
Supply voltage		tage				ige		age		ltage		-0.5~+7.0	V
Input/output voltage			V _I , V _O	-0.5~V _{CC} +0.5	V								
Input protect	ion diode current		I_{IK}	±20	mA								
Output parasitic diode current			I _{OK}	±20	mA								
Output current			I_{O}	±25	mA								
Supply curren	nt		I _{CC} , I _{GND}	±50	mA								
Storage temp	erature range		Tstg	−65~+150	°C								
	MN74HCT377	Ta=-40~+60°C	P _D	400	mW								
Power	WIN74HC1377	Ta=+60~+85°C	I ID	Decrease to 200mW at the rate of 8mW/°C	11144								
dissipation	MN74HCT377S	Ta=-40~+60°C	P _D	275	mW								
	WIN74HC13773	Ta=+60~+85°C	I D	Decrease to 200mW at the rate of 3.8mW/°C	11144								

■ Operating Conditions

Parameter	Symbol	V _{cc} (V)	Rating	Unit
Operating supply voltage	V _{cc}		4.5~5.5	V
Input/output voltage	V _I , V _O		0∼V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
Input rise and fall time	t _r , t _f	V _{CC} =4.5V	0~500	ns

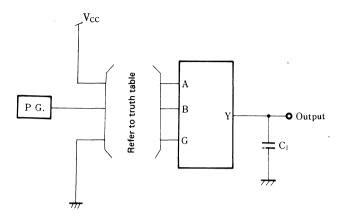
	Symbol	V _{cc} (V)	Test Conditions		Temperature						
Parameter			$V_{\rm I}$	T.	I _O	Ta=25°C			Ta = -40	~+85°C	Unit
			V _I	10	Unit	min.	typ.	max.	min.	max.	
		4.5									
Input HIGH voltage	V _{iH}	≀				2.0			2.0		V
		5.5									
		4.5								i	
Input LOW voltage	V _{IL}	≀						0.8		0.8	V
		5.5									
		4.5	V _{IH}	-20.0	μΑ	4.4	4.5		4.4		v
Output HIGH voltage	V_{OH}		or								
		4.5	V _{IL}	-4.0	mA	3.86			3.76		V
		4.5	V _{IH}	20.0	μΑ		0.0	0.1		0.1	V
Output LOW voltage	V_{OL}		or								
		4.5	V_{IL}	4.0	mA			0.32		0.37	V
Input current	I_{I}	5.5	V_{I} =	V _{CC} or G	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	5.5	$V_I = V_{CC}$	or GND	$I_0=0$	•		8.0		80.0	μΑ

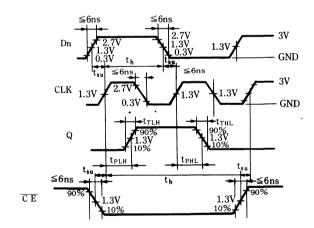
■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C_L=50pF)

		.,		L	T	emperatu	re		1
Parameter	Symbol	(V)	Test Conditions		Ta=25°C		Ta=-40	~+85°C	Unit
		ì.		mın.	typ.	max.	min.	max.	
Output rise time	t _{TLH}	4.5				15		19	ns
Output fall time	t _{THL}	4.5		·		15		19	ns
Propagation time CLK→D (L→H)	t _{PLH}	4.5				30		38	ns
Propagation time CLK→D (H→L)	t _{PHL}	4.5				30		38	ns
Minimum Set-up time D	t _{su}	4.5				20		25	ns
Minimum Set-up time CE	t _{su}	4.5				20		25	ns
Minimum Hold time D	t _h	4.5				. 0		0	ns
Minimum Hold time CE	t _h	4.5				0		0	ns
Minimum pulse width CLK	t _w	4.5				20		25	ns
Maximum clock frequency	f _{max}	4.5		30			24		MHz



- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})





MN74HC386/MN74HC386S

Quad 2-Input Exclusive OR Gates

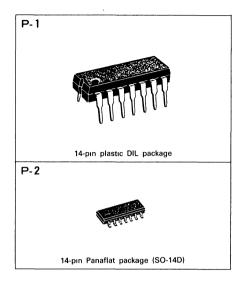
■ Description

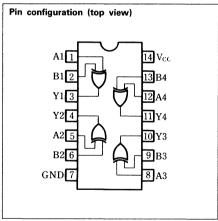
MN74HC386/MN74HC386S contain quad 2-input exclusive OR gates.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directry driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

■ Logic Diagram (1 gate)







■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit	
Supply voltage			Vcc	−0.5~+7.0	V	
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V	
Input protec	tion diode current		Iıĸ	±20	mA	
Output parasitic diode current			Іок	±20	mA	
Output current			Io	±25	mA	
Supply curre	ent		Icc, IGND	±50	mA	
Storage tem	perature range		Tstg	-65~+150	${\mathcal C}$	
	MN74HC386	Ta=-40~+60°C	P_{D}	400	m W	
Power	MIN74HC360	Ta=+60~+85 ℃	F))	Decrease to 200mW at the rate of 8mW/°C		
dissipation	MN74HC386S	Ta=-40~+60℃	D	275	117	
	MIN/4HC360S	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m W	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V ₁ , V ₀		0~Vcc	v
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

	Symbol		Те	st Conditi	ons		Te	emperat	ure		
Parameter		V _{CC} (V)	Vı	Τ	Ta=25℃			Ta=-40~+85℃		Unit	
		(*)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5		ļ		3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{IL}	4.5			,			0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	Vон	4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μΑ	5.9	6.0		5.9		v
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	Vin	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V _{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	Icc	6.0	$V_I = V_0$	c or GNI	O, I _O =0			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

		T	Test Conditions						
Parameter	Symbol	(V)			Ta=25°	2	Ta=-40)~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5		İ	7	15		19	ns
		6.0			6	13		16	
		2.0			25	75		95	
Propagation time (L → H)	t PLH	4.5			8	15		19	ns
(L · II)		6.0			7	13		16	
	t _{PHL}	2.0			25	75		95	
Propagation time $(H \rightarrow L)$		4.5			8	15		19	ns
(11 - 11)		6.0			7	13		16	

MN74HC390/MN74HC390S

Dual 4-Bit Decade Counters

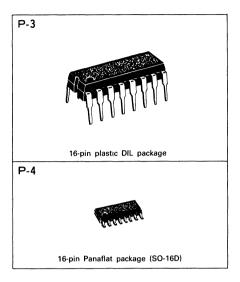
■ Description

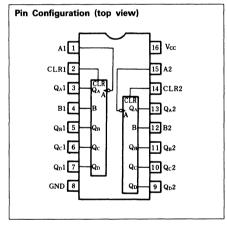
MN74HC390/MN74HC390S are independent ripple-carry counters consisting of two decade counters.

The decade counter consists of divide-by-two and divide-by-five counters. Divide-by-two and divide-by-five counters can have a maximum of divide-by-100 counters by using two decade counters or combinations.

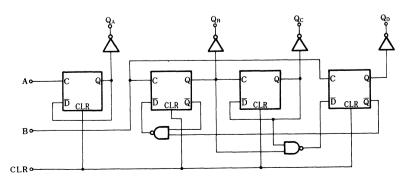
This counter provides increments on the negative-going edge of clock input, and each has independent clear input. When the clear input is HIGH, all of the four outputs of each counter become LOW. The clear input decreases the count number and functions to make this counter a Modulo-N counter.

Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.





■ Logic Diagram



■ Truth Table

A or B	CLR	Output
×	Н	L
7	Ī.	Count

Note

1. ×: Either HIGH or LOW; it doesn't matter 2. \(\gamma\): A(B) from "H" to "L"

* Output QA to be connected to input B

Count	Output								
Count	\mathbf{Q}_{D}	\mathbf{Q}_{C}	Q_B	Q _A					
0	L	L	L	L					
1	L	L	L	Н					
2	L	L	Н	L					
3	L	L	Н	Н					
4	L	Н	L	L					
5	L	Н	L	Н					
6	L	Н	Н	L					
7	L	Н	Н	Н					
8	Н	L	L	L					
9	Н	L	L	Н					

\divideontimes Output Q_D to be connected to input A

Count		Out	put	
Count	Q_A Q_D		$Q_{\rm C}$	Q_B
0	L	L	L	L
1	L	L	L	Н
2	L	L	Н	L
3	L	L	Н	Н
4	L	. Н	L	L
5	Н	L	L	L
6	Н	L	L	Н
7	Н	L	Н	L
8	Н	L	Н	Н
9	Н	Н	L	L

■ Absolute Maximum Ratings

	Paramete	er	Symbol	Rating	Unit	
Supply voltage			Vcc	$-0.5 \sim +7.0$	V	
Input/output	voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V	
Input protection diode current			I _{IK}	±20	mA	
Output paras	sitic diode current		Іок	±20	mA	
Output current			Io	± 25	mA	
Supply curre	ent		Icc, IGND	±50	mA	
Storage tem	perature range		Tstg	−65~+150	$^{\circ}\mathbb{C}$	
	MN74HC390 Ta=−40~+60°C Pn	MN74HC200 Ta=−40~+60°C	400	337		
Power	MN74HC390	Ta=+60~+85℃	P _D	Decrease to 200mW at the rate of 8mW/°C	m W	
dissipation MN74HC390S		Ta=-40~+60℃	D	275	m W	
		Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m W	

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	Vcc		$1.4 {\sim} 6.0$	V
Input/output voltage	V_{I}, V_{O}		0~Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		.,,	Te	st Condition	ons		Т	emperat	ure		
Parameter	Symbol	(V)	Vı	Io		Ta=25 °C			Ta=-40~+85°C		Unit
			VI	10	Unit	min.	typ.	max.	mın.	max.	
Input HIGH voltage		2.0				1.5			1.5		
	V _{IH}	4.5				3.15			3.15		V
		6.0		i i		4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V11	4.5						0.9		0.9	V
		6.0		1				1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	Vон	4.5	Vih	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V _{II} .	-4.0	mA	3.86			3.76.		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1	1	0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	Icc	6.0	$V_I = V_C$	c or GNI	$I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

					Т	empera	ture		
Parameter	Symbol	V _{CC} (V)	Test Conditions	,	Ta=25℃	2	Ta=-40)~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15		19	ns
		6.0				13		16	
		2.0				150		190	
Propagation time	t PLH	4.5			17	30	1	38	ns
$A \rightarrow Q_A (L \rightarrow H)$		6.0				26		33	
		2.0				125		155	
Propagation time	t PHL	4.5			15	25		31	ns
$A \rightarrow Q_A (H \rightarrow L)$		6.0				21		26	
D (' 1'		2.0				325		406	
Propagation time	t PLH	4.5			38	65		81	ns
$A \rightarrow Q_C (L \rightarrow H)$		6.0				55		69	
		2.0				325		406	
Propagation time	t PHL	4.5			38	65		81	ns
$A \rightarrow Q_C (H \rightarrow L)$		6.0				55		69	

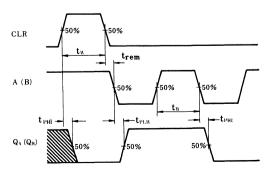
■ AC Characteristics (Cont'd)

					Te	mperat	ure		
Parameter	Symbol	Vcc	Test Conditions	•	Ta=25°	2	Ta=-40)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
Propagation time		2.0				175		220	
$B \rightarrow Q_B (L \rightarrow H)$	t PLH	4.5			22	35		44	ns
D→ØB (L→U)		6.0				30		37	
Propagation time		2.0				150		190	
	t PHL	4.5			18	30		38	ns
$B \rightarrow Q_B (H \rightarrow L)$		6.0		1	1	26		33	
Dana and in dia.		2.0				200		250	
Propagation time	t PLH	4.5		}	24	40		50	ns
$B \rightarrow Q_C (L \rightarrow H)$		6.0				34		43	
D		2.0				200		250	
Propagation time	t PHL	4.5		İ	24	40		50	ns
B→Q _c (H→L)		6.0				34		43	
D		2.0				. 175		220	
Propagation time	t PLH	4.5			20	35		44	ns
$B \rightarrow Q_D (L \rightarrow H)$		6.0				30		37	
D		2.0				150		190	
Propagation time	t PHL	4.5		ļ	17	30		38	ns
$B \rightarrow Q_D (H \rightarrow L)$		6.0		1		26		33	
D		2.0				175		220	
Propagation time	t PHL	4.5			20	35		44	ns
$CLR \rightarrow Q (H \rightarrow L)$		6.0				30		37	
		2.0				125		155	
Minimum pulse width	t w	4.5			5	25		31	ns
CLK(A),CLK(B),CLR		6.0				21		26	
		2.0				75		95	
Minimum recovery time	trem	4.5			3	15		19	ns
·		6.0	•			13		16	
		2.0		6			4		
Maximum clock frequency	fmax	4.5		30	81		24		MHz
A, B		6.0		35			28		

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit Vcc P. G. Qa CLR A QB CI TCI TT GND Output CI TT Output CI TT Output CI TT Output TCI TT Output TCI TT Output TCI TT Output TCI TT Output TCI TT Output

2. Waveforms



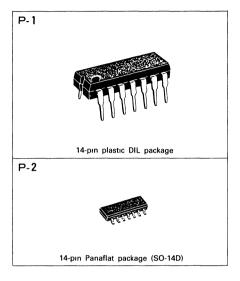
MN74HC393/MN74HC393S

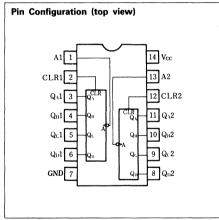
Dual 4-Bit Binary Counters

■ Description

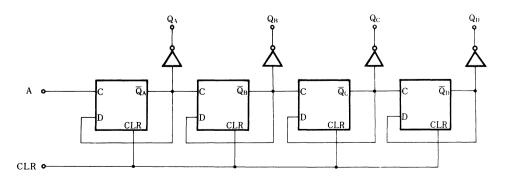
MN74HC393/MN74HC393S are independent ripple-carry counters consisting of two independent 4-bit ripple-carry binary counters which can be subsidiarily connected to one divide-by-256 counter.

This counter provides increments on the negative-going edge of clock input, and each has independent clear input. When the clear input is HIGH, all of the four outputs of each counter become LOW. The clear input decrease the count number and functions to make this counter a Modulo-N counter. Adoption of a silicon gate CMOS process has realized a low power dissipation, high noise margin equivalent to a standard CMOS and operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family. family.





■ Logic Diagram





	Paramete	r	Symbol	Rating	Unit		
Supply voltage	upply voltage		y voltage		Vcc	$-0.5 \sim +7.0$	V
Input/output voltage			V_1 , V_0	$-0.5 \sim V_{CC} + 0.5$	V		
Input protection diode current			Iıĸ	±20	mA		
Output parasitic diode current			Іок	±20	mA		
Output current			Ιο	±25	mA		
Supply curre	y current		Icc, IGND	±50	mA		
Storage tem	e temperature range		nperature range		Tstg	-65~+150	$^{\circ}$
	MN74HC393	Ta=-40~+60°C	P_{D}	400	***		
Power	MN74HC393	Ta=+60~+85℃	F)	Decrease to 200mW at the rate of 8mW/°C	mW		
dissipation	·		P_{D}	275	. 11/		
	MN74HC393S Ta=+60~+85℃		P)	Decrease to 200mW at the rate of 3.8mW/°C	m W		

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V _I , V _O		$0 \sim V_{\rm CC}$	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

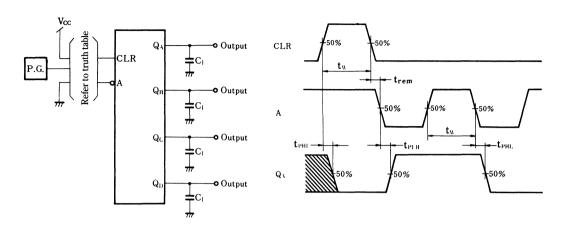
			Te	st Condition	ons		T	emperat	ure		
Parameter	Symbol	Vcc	37	T		Γa=25 °	C	Ta=-40	~+85℃	Unit	
		(V)	Vi	Io	Unit	mın.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15	į	V
		6.0				4.2			4.2	ŀ	
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
	Ýон	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	Vih	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76	1	
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I _i	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
Quiescent supply current	$I_{\rm CC}$	6.0	$V_I = V_C$	c or GNI), I ₀ =0			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

					Te	mperati	ure		
Parameter	Symbol	(V)	Test Condition		Ta=25 °	2	Ta=-40)~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0			20	75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
,		6.0			7	13		16	
		2.0			15	75		95	
Output fall time	t _{THL}	4.5			8	15		19	ns
	-	6.0			7	13		16	
_		2.0			27	100		120	
Propagation time	t _{PLH}	4.5			12	20		24	ns
$A \rightarrow Q_A (L \rightarrow H)$		6.0			9	17		20	
		2.0			24	100		120	
Propagation time	t _{PHL}	4.5		1	10	20	1	24	ns
$A \rightarrow Q_A (H \rightarrow L)$		6.0			9	17		20	
-		2.0			53	175		220	
Propagation time	t _{PLH}	4.5			22	35		44	ns
$A \rightarrow Q_D (L \rightarrow H)$		6.0		1	15	30		37	
D		2.0			53	175		220	
Propagation time	t PHL	4.5			22	35		44	ns
$A \rightarrow Q_D (H \rightarrow L)$		6.0			15	30		37	
D		2.0			33	150		190	
Propagation time	t _{PHL}	4.5			17	30		38	ns
$CLR \rightarrow Q (H \rightarrow L)$		6.0			14	26		33	
		2.0			16	75		95	
Mınımum pulse wıdth	t w	4.5			18	15		19	ns
CLK, CLR		6.0			7	13		16	
		2.0			10	, 75		95	
Minimum Set-up time	trem	4.5			4	15		19	ns
		6.0			3	13		16	
****		2.0		6	38		5		
Maximum clock frequency	f _{max}	4.5		30	68		24		MHz
•		6.0		35	98		28		



- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})



■ Truth Table

A	CLR	Output
×	Н	L
7	L	Count

Note:

1. ×: Either HIGH or LOW; it doesn't matter

2. \nearrow : count on the negative-going edge from HIGH to LOW of

Count		Out	put	
Count	\mathbf{Q}_{D}	$Q_{\rm C}$	Q_B	Q _A
0	L	L	L	L
1	L	L	L	Н
2	L	L	Н	L
3	L	L	Н	Н
4	L	Н	L	L
5	L	Н	L	Н
6	L	Н	Н	L
7	L	Н	Н	Н
8	Н	L	L	L
9	Н	L	L	Н
10	Н	L	Н	L
11	Н	L	Н	Н
12	Н	Н	L	L
13	Н	Н	L	Н
14	Н	Н	Н	L
15	Н	Н	Н	Н

MN74HC533/MN74HC533S

Octal TRI-STATE D-Type Latches with Inverting Outputs

■ Description

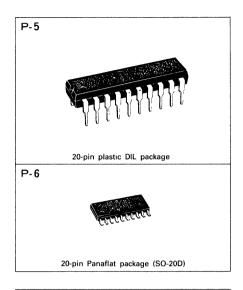
MN74HC533/MN74HC533S contain eight high-speed D-type latches with inverting tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system.

When output disable input is LOW and latch enable input is HIGH, the output outputs the inverting data input state.

When latch enable is LOW, the data input data is held in the output until when latch enable input becomes HIGH.

When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.



■ Truth Table

Output Control	Enable G	D	Output
L	Н	Н	L
L	Н	L	Н
L	L	×	Q _o
Н	×	×	Hi-Z

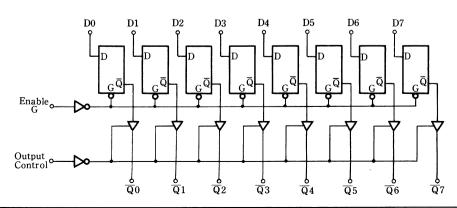
Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance
- 3. Q_0 : Q level prior to determination of input condition shown in tabel

OC 1 20 Vcc Q0 2 c 19 Q7 D0 3 c 19 Q7 D1 4 c 17 D6 Q1 5 c 2 6 c 2 6 C 2

Pin Configuration (top view)

■ Logic Diagram



Parameter			Symbol	Rating	Unit
Supply voltage			Vcc	$-0.5 \sim +7.0$	V
Input/output voltage			V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protection diode current			I_{1K}	±20	mA
Output parasitic diode current			Іок	± 20	mA
Output current			Ιο	± 35	mA
Supply current			Icc, IGND	±70	mA
Storage temperature range			Tstg	-65~+150	$^{\circ}$
	MN74HC533	Ta=-40~+60℃	P_{D}	400	mW
Power	Ta=+60~+85℃	I (1)	Decrease to 200mW at the rate of 8mW/°C	m vv	
dissipation M	MN74HC533S	Ta=-40~+60℃	D	275	m W
	WW/4HC5335	Ta=+60~+85°C	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

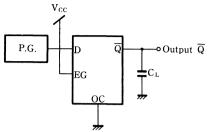
Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	$V_{\rm I}, V_{\rm O}$		0~Vcc	V
Operating temperature range	TA		$-40 \sim +85$	r
Input rise and fall time		2.0	0~1000	ns
	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

Parameter	Symbol	V _{cc} (V)	Test Conditions		Temperature						
			Vı	Io [Ta=25℃		2	Ta=-40~+85 °C		Unit
					Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	VIL	4.5						0.9		0.9	V
		6.0						1.2		1.2	
	Vон	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V _{IL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
	Vol	2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state current	Ioz	6.0	V _I =V _{IH} or V _{IL}				±0.5		±5.0	μΑ	
			Vo=Vcc or GND				±0.5		_ ±3.0	μΑ	
Quiescent supply current	I_{CC}	6.0	$V_1 = V_0$	cc or GNI	$I_0=0$			8.0		80.0	μA

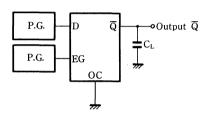
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

Parameter	Symbol	V _{cc} (V)	Test Conditions	Temperature					
				Ta=25 ℃			Ta=-40)~+85℃	Unit
				min.	typ.	max.	min.	max.	
Output rise time		2.0			7	75		95	
	t _{TLH}	4.5				15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t THL	4.5		-	6	15		19	ns
		6.0				13		16	
Propagation time		2.0				100		125	
$D \rightarrow \overline{Q} (L \rightarrow H)$	t PLH	4.5			13	20		25	ns
D→Q (L→n)		6.0		1		17	}	21	
D		2.0				100		125	
Propagation time	t PHL	4.5			12	20		25	ns
$D \rightarrow \overline{Q} (H \rightarrow L)$		6.0				17		21	
		2.0	Annual Control of the			125		155	ns
Propagation time	t PLH	4.5			14	25		31	
Enable $G \rightarrow \overline{Q}(L \rightarrow H)$	1 21 211	6.0				21		26	
	t _{PHL}	2.0				125		155	
Propagation time		4.5	1		15	25		31	ns
Enable $G \rightarrow \overline{Q}(H \rightarrow L)$		6.0				21		26	
	t _{PHZ}	2.0		1		125		155	
3-state propagation time		4.5	$R_L = 1 k\Omega$	14	25		31	ns	
$(H \rightarrow Z)$		6.0				21		26	
	t _{PLZ}	2.0				125		155	
3-state propagation time		4.5	$R_L = 1 k\Omega$		10	25		31	ns
$(L \rightarrow Z)$		6.0				21	1	26	
		2.0				100		125	ns
3-state propagation time	t _{PZH}	4.5	$R_L = 1 k\Omega$		10	20		25	
(Z→ H)		6.0				17		21	
		2.0				100		125	
3-state propagation time	t PZL	4.5	$R_L = 1 k\Omega$		12	20		25	ns
(Z→L)	CPZI.	6.0				17		21	
Minimum Set-up time	t _{su}	2.0				75	†	95	
		4.5			6	15		19	ns
		6.0				13		16	5
Minimum Hold time		2.0			_	0		0	
	ld time t _h	4.5			_	0		0	ns
		6.0			_	0		0	
	L	L 5.0	<u> </u>				<u> </u>		

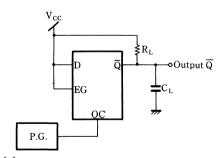
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , $t_{PLH}/t_{PHL}(D \rightarrow \overline{Q})$
 - 1. Measuring Circuit



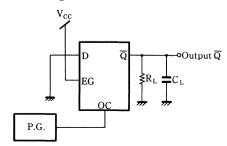
- (2) $t_{PLH}/t_{PHL}(EG \rightarrow \overline{Q})$, t_{su}
 - 1. Measuring Cırcuit

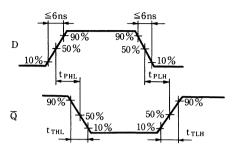


- $(3)t_{PHZ}, t_{PZH}$
 - 1. Measuring Circuit

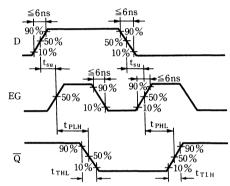


- (4) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit

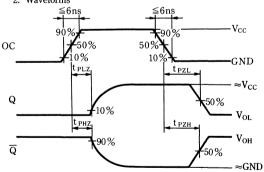




2. Waveforms



2. Waveforms



2. Waveforms

See above [3] 2. for waveforms.

MN74HC534/MN74HC534S

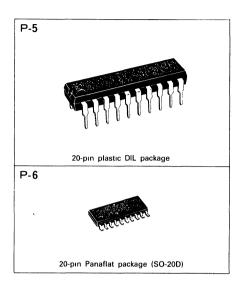
Octal TRI-STATE D-Type Flip-Flops with Inverting Outputs

■ Description

MN74HC534/MN74HC534S contain eight high-speed D-type flipflops with inverting tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system. D input data satisfying set-up time is inverted and transferred to the output on the positive going edge of clock input.

When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.



■ Truth Table

	Input						
Output Control	CLK	D	$\overline{\overline{Q}}$				
L	5	Н	L				
L	5	L	Н				
L	L	×	$\overline{\overline{Q}}_{o}$				
Н	×	, ×	Hi-Z				

Note: 1. ____:

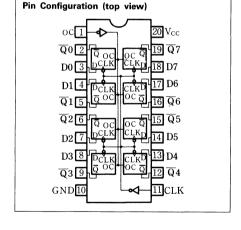
Data input is transferred to output on the negative-going edge from LOW to HIGH of the clock

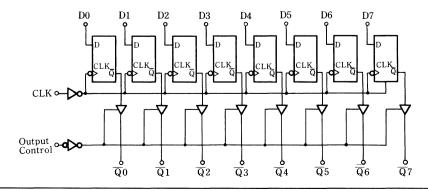
2. x: Either HIGH or LOW; it doesn't matter

3. Q_O: Q level prior to determination of input condition shown in

table

4. Hi-Z: High impedance





	Paramete	r	Symbol	Rating	Unit																	
Supply volta	Supply voltage			$-0.5 \sim +7.0$	V																	
Input/output	Input/output voltage			output voltage		ut/output voltage		t/output voltage		ıt/output voltage		tput voltage		itput voltage		output voltage		output voltage		V_1, V_0	$-0.5 \sim V_{CC} + 0.5$	V
Input protec	Input protection diode current			± 20	mA																	
Output paras	Output parasitic diode current			± 20	mA																	
Output curre	Output current			±35	mA																	
Supply curre	rrent		Icc, I _{GND}	±70	mA																	
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$																	
	MN74HC534	Ta=-40~+60°C	Pp	400	14/																	
Power	MIN7411C554	$T_a = +60 \sim +85 ^{\circ}$		Decrease to 200mW at the rate of 8mW/°C	m W																	
dissipation	dissipation MN74HC534S	Ta=-40~+60℃	Po	275	W																	
	WIN/4/IC5545	Ta=+60~+85℃	r ₍₎	Decrease to 200mW at the rate of 3.8mW/°C	m W																	

■ Operating Conditions

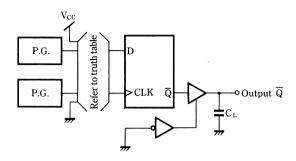
Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0∼Vcc	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r ,t _f	4.5	0~500	ns
		6.0	0~400	ns

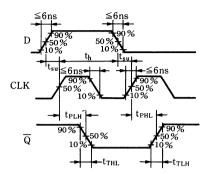
		$V_{\rm cc}$	Те	st Conditi	ons		Te	mperati	ıre			
Parameter	Symbol	(V)	Vı	Io		•	Ta=25 °	C	Ta=-40)~+85 ℃	Unit	
		(v)	• 1	10	Unit	min.	typ.	max.	min.	max.		
Input HIGH voltage		2.0				1.5			1.5			
	V _{IH}	4.5				3.15			3.15		V	
		6.0				4.2		Ì	4.2			
		2.0						0.3		0.3		
Input LOW voltage	VIL	4.5						0.9		0.9	V	
		6.0						1.2		1.2		
		2.0		-20.0	μΑ	1.9	2.0		1.9			
		4.5	VIH	-20.0	μA	4.4	4.5		4.4			
Output HIGH voltage	Von	6.0	or	-20.0	μA	5.9	6.0		5.9		V	
		4.5	VIL	-6.0	mA	3.86			3.76			
		6.0		-7.8	mA	5.36			5.26			
		2.0		20.0	μΑ		0.0	0.1		0.1		
		4.5	Vih	20.0	μA		0.0	0.1		0.1		
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V	
		4.5	VIL	6.0	mA			0.32		0.37		
		6.0		7.8	mA			0.32		0.37		
Input current	Iı	6.0	$V_I = V$	cc or G	ND			±0.1		±1.0	μA	
3-state output off state	,	6.0	$V_1 = V$	in or V	IL			+0.5		+50		
current	Ioz	6.0	Vo=Vcc or GND				±0.5		±5.0	μΑ		
Quiescent supply current	Icc	6.0	$V_{I} = V_{C}$	c or GNI	$I_0=0$			8.0		80.0	μΑ	

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

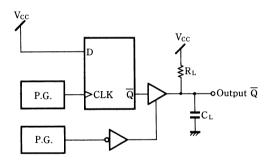
		.,			Temper	ature C	ondition	ı	
Parameter	Symbol	Vcc	Test Conditions	,	Ta=25°	2	Ta=-40	~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13	İ	16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0							
$CLK \rightarrow \overline{Q} (L \rightarrow H)$	t PLH	4.5			17	30			ns
OER 'Q (E 'II)		6.0							
D		2.0				125		155	
Propagation time	t PHL	4.5			15	25		31	ns
$CLK \rightarrow \overline{Q} (H \rightarrow L)$		6.0				21		26	
3-state propagation time		2.0				150		190	
(H→Z)	t _{PHZ}	4.5	$R_L=1k\Omega$		17	30		38	MHz
(n→ 2)		6.0				26		33	
3-state propagation time		2.0				150		190	
(L→Z)	t PLZ	4.5	$R_L=1k\Omega$		17	30		38	ns
(L→Z)		6.0				26		33	
3-state propagation time		2.0				100		125	
(Z→H)	t _{PZH}	4.5	$R_L=1k\Omega$		12	20		25	ns
(Z→11)		6.0				17		21	
0 -1-1		2.0				100		125	
3-state propagation time	t _{PZL}	4.5	$R_L=1k\Omega$		13	20		25	ns
(Z→L)		6.0				17		21	
		2.0				100		125	
Minimum Set-up time	tsu	4.5			2	20		25	ns
		6.0				17		21	
		2.0				0		0	
Minimum Hold time	th	4.5				0		0	ns
		6.0				0		0	
		2.0		6			4		
Maximum clock frequency	fmax	4.5		30	49		24		ns
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , $t_{PLH}/t_{PHL}(CLK \rightarrow \overline{Q})$, t_{su} , t_{max} , t_h
 - 1. Measuring Circuit

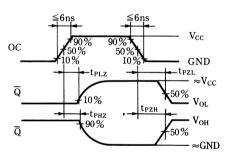




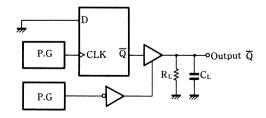
- (2) t_{PHZ}, t_{PZH}
 - 1. Measuring Circuit



2. Waveforms



- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

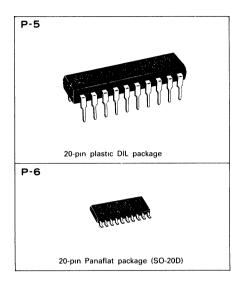
MN74HC540/MN74HC540S

Inverting Octal TRI-STATE Buffers Line Drivers

■ Description

MN74HC540/MN74HC540S are inverting octal tri-state buffers line drivers. Large current output make possible high-speed operation for driving a large capacity bus line. When one of 3-state control input $(\overline{G1}, \overline{G2})$ operated as 2 inputs NOR is "H", 8 outputs become high impedance.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



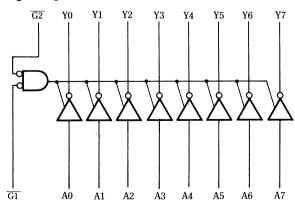
■ Truth Table

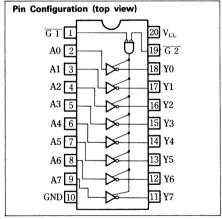
	Input		Output
G ₁	G ₂	An	Yn
L	L	L	Н
L	L	Н	L
×	Н	×	Z
Н	×	×	Z

Note:

1. ×: Either HIGH or LOW; doesn't matter

2. Hi-Z: Hi-Impedance





	Paramet	er	Symbol	Rating	Unit		
Supply voltage	Supply voltage			-0.5~+7.0	V		
Input/output voltage			V _I , V _O	-0.5~V _{CC} +0.5	V		
Input protect	ion diode current		I _{IK} ±20				
Output paras	Output parasitic diode current			±20	mA		
Output curre	Output current			±35	mA		
Supply curre	urrent		rent		I _{CC} , I _{GND}	±70	mA
Storage temp	erature range		Tstg	−65~+150	°C .		
	MN74HC540	Ta=-40~+60°C	P_{D}	400	mW		
Power	WIN74HC540	Ta=+60~+85°C		Decrease to 200mW at the rate of 8mW/°C	111 44		
dissipation	MN74HC540S	Ta=-40~+60°C	P _D	275	mW		
	WIN7411C5405	Ta=+60~+85°C	r _D	Decrease to 200mW at the rate of 3.8mW/°C	111 VV		

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output	V _I , V _O		0∼V _{CC}	V
Operating temperature range	T _A		−40~+85	°C
Input rise and fall time		V _{CC} =2.0V	0~1000	ns
	t_r , t_f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0V	0~400	ns

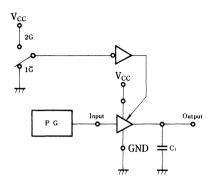
			Tes	t Conditio	ons		Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vī	T	T		Ta=25°C		Ta=-40	~+85°C	Unit
		(,,	V _I	$I_{\rm O}$	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5	i		1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	V
		2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V _{IH}	-20.0	μΑ	4.4	4.5		4.4		V
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	-6.0	mA	3.86		ļ	3.76		V V V V V V V
		6.0		-7.8	mA	5.36			5.26		V
		2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V _{IH}	20.0	μΑ		0.0	0.1	İ	0.1	v
Output LOW voltage	V_{OL}	6.0	or	20.0	μΑ		0.0	0.1		0.1	V V V V V V V V V V V V V V V V V V V
		4.5	V_{IL}	6.0	mA			0.32		0.37	
	1	6.0	1	7.8	mA	ļ		0.32		0.37	V
Input current	Iı	6.0	V _I =	V _{CC} or G	ND			±0.1		±1.0	μA
3-state output off state current	I _{OZ}	0.6		V _{IH} or V V _{CC} or C				±0.5		±5.0	μA
Quiescent supply current	I _{CC}	6.0	$V_I = V_{CC}$	or GND	, $I_0=0$			8.0		80.0	μΑ

■ AC Characteristics (GND=0V, Input transistion tiem \leq 6ns, C_L =50pF)

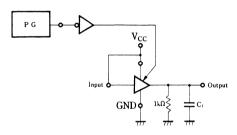
					T	emperatu	re		
Parameter	Symbol	V _{CC} (V) Test Condition			Ta=25°C		Ta = -40	~+85°C	Unit
		(.,		min.	typ.	max.	min.	max.	
		2.0			28	75		95	
Output rise time	t _{TLH}	4.5			12	15		19	ns
		6.0			10	13	Ì	16	
		2.0			22	75		95	
Output fall time t	t _{THL}	4.5			9	15		19	ns
		6.0			7	13	ĺ	16	
D		2.0			39	90		115	
Propagation time (L→H)	t _{PLH}	4.5			14	18		23	ns
		6.0			12	15		20	
_		2.0			40	90		115	
Propagation time (H→L)	t _{PHL}	4.5			14	18	1	23	ns
(az · 2)		6.0			11	15		20	
3-stage output off		2.0			46	140		175	
leakage current	t_{PHZ}	4.5	$R_L = 1k\Omega$		22	28	1	35	ns
(H→Z)		6.0			19	24]	30	
3-stage output off		2.0			44	140		175	
leakage current	t _{PLZ}	4.5	$R_L = 1k\Omega$		17	28		35	ns
(L→Z)		6.0			19	24		30	
3-stage output off		2.0			62	140		175	
leakage current	t _{PZH}	4.5	$R_L = 1k\Omega$		23	28		35	ns
(Z→H)		6.0			18	24		30	
3-stage output off		2.0			62	140		175	
leakage current	t _{PZL}	4.5	$R_L = 1k\Omega$		23	28		35	ns
(Z→Ľ)	1	6.0			18	24		30	

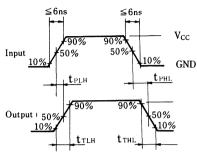


- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , t_{PLH} , t_{PHL}
 - 1. Measuring Circuit

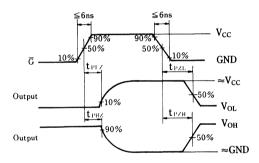


- (2) t_{PHZ}, t_{PZH}
 - 1. Measuring Circuit

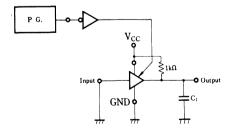




2. Waveforms (tphz, tpzh, tplz, tpzl)



- (3) t_{PLZ}, t_{PZL}
 - 1. Measuring Circuit



MN74HC541/MN74HC541S

Octal TRI-STATE Buffers Line Drivers

■ Description

MN74HC541/MN74HC541S are octal tri-state buffers line drivers. Large current output make possible high-speed operation for driving a large capacity bus line. When one of 3-state control input $(\overline{G}1,\overline{G}2)$ operated as inputs NOR is "H". 8 outpurs become high impedance

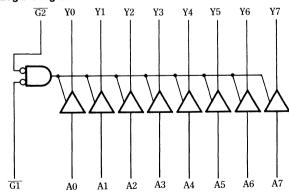
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

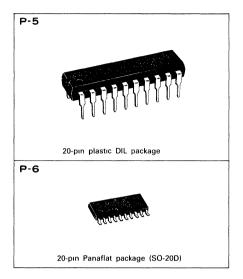
■ Truth Table

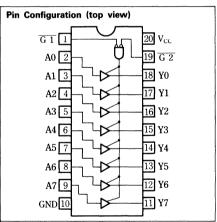
	Input		Output
G1	G2	An	Yn
L	L	L	Н
L	L	Н	L
×	Н	×	Z
Н	×	×	Z

Note:

- 1. x: Either HIGH or LOW; doesn't matter
- 2. Hi-Z: Hi-Impedance









	Paramete	er	Symbol	Rating	Unit				
Supply voltage			V _{cc}	-0.5∼+7.0	V				
Input/output voltage			V _I , V _O	-0.5~V _{CC} +0.5	V				
Input protect	ion diode current		I _{IK} ±20						
Output parasi	tic diode current	ent I _{OK} ±20							
Output curre	nt		Output current			I _O ±35			
Supply curren	nt	I_{CC} , I_{GND} ± 70			mA				
Storage temp	erature range		Tstg	−65~+150	°C				
	MN74HC541	Ta=-40~+60°C	P_{D}	400	mW				
Power	MIN74HC541	Ta=+60~+85°C	I D	Decrease to 200mW at the rate of 8mW/°C	11177				
dissipation	MN74HC541S	Ta=-40~+60°C	P_{D}	275	mW				
	WIN7411C3413	Ta=+60~+85°C	I D	Decrease to 200mW at the rate of 3.8mW/°C	111 44				

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0∼V _{CC}	V
Operating temperature range	T _A		−40~+85	°C
		V _{CC} =2.0V	0~1000	ns
Input rise and fall time	t _r , t _f	V _{CC} =4.5V	0~500	ns
		V _{CC} =6.0V	0~400	ns

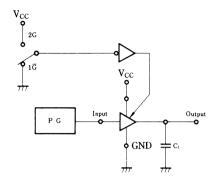
			Tes	t Conditio	ons		T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	17	т			Ta=25°C		Ta=-40	~+85°C	Unit
	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$										
		2.0				1.5			1.5		V
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		V
		2.0						0.3		0.3	V
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	V
		2.0		-20.0	μΑ	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μΑ	4.4	4.5		4.4		V
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	V_{IL}	±6.0	mA	3.86			3.76		V
		6.0		-7.8	mA	5.36			5.26		V
		2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
Output LOW voltage	V_{OL}	6.0	or	20.0	μΑ		0.0	0.1		0.1	V
		4.5	V _{IL}	6.0	mA			0.32		0.37	V
		6.0	Ì	7.8	mA			0.32		0.37	V
Input current	II	6.0	V _I =V _{CC} or GND				±0.1		±1.0	μΑ	
3-state output off state current	I_{OZ}	0.6	$V_{I} = V_{O} =$	=V _{IH} or V V _{CC} or G	I _{IL} SND			±0.5		±5.0	μΑ
Quiescent supply current	Icc	6.0	$V_I = V_{CC}$	or GND	$I_{O}=0$			8.0		80.0	μΑ

■ AC Characteristics (GND=0V, Input transistion tiem \leq 6ns, C_L=50pF)

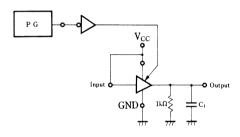
	1				Temperature						
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta=-40)~+85°C	Unit		
				min.	typ.	max.	min.	max.			
		2.0			27	75		95			
Output rise time	t _{TLH}	4.5			12	15	ļ	19	ns		
		6.0			10	13		16			
		2.0			26	· 75		95			
Output fall time	t _{THL}	4.5			10	15		19	ns		
		6.0			7	13		16			
D		2.0			33	90		115			
Propagation time (L→H)	t_{PLH}	4.5			13	18		23	ns		
<u> </u>		6.0			11	15		20			
		2.0			36	90		115			
Propagation time (H→L)	t _{PHL}	4.5			13	18		23	ns		
		6.0			10	15		20			
3-stage output off		2.0			42	140		175			
leakage current	t _{PHZ}	4.5	$R_L = 1k\Omega$		23	28		35	ns		
$(H \rightarrow Z)$		6.0			20	24		30			
3-stage output off		2.0			40	140		175			
leakage current	t_{PLZ}	4.5	$R_L = 1k\Omega$		16	28		35	ns		
(L→Z)		6.0			13	24		30			
3-stage output off		2.0			59	140		175			
leakage current	t _{PZH}	4.5	$R_L = 1k\Omega$		21	28		35	ns		
(Z→H)		6.0			17	24	ĺ	30			
3-stage output off		2.0			63	140		175			
leak current	t_{PZL}	4.5	$R_L = 1k\Omega$		22	28		35	ns		
$(Z \rightarrow L)$		6.0			17	24		30			



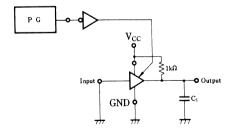
- · Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , t_{PLH} , t_{PHL}
 - 1. Measuring Circuit

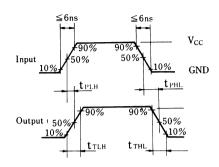


- (2) t_{PHZ}, t_{PZH}
 - 1. Measuring Circuit

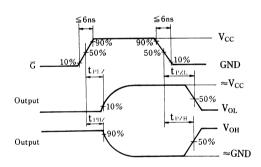


- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit





2. Waveforms (tphz, tpzh, tplz, tpzl)



MN74HC563/MN74HC563S

Octal TRI-STATE D-Type Latches with Inverting Outputs

■ Description

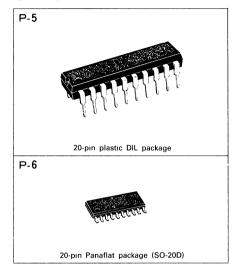
MN74HC563/MN74HC563S contain eight high-speed D-type latches with inverting tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system.

When output disable input is LOW and latch enable input is HIGH, the output outputs the inverting data input state.

When latch enable is LOW, the data input is held in the output until when latch enable input becomes HIGH.

When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.



■ Truth Table

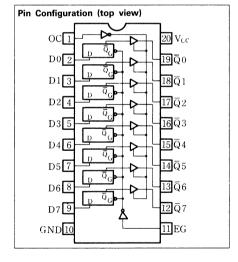
	Input		Output
Output Control	Enable G	D	Q
L	Н	Н	L
L	Н	L	Н
L	L	×	$\overline{Q}_{\mathrm{O}}$
Н	×	×	Hi-Z

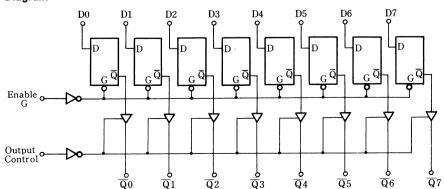
Note:

1. ×: Either HIGH or LOW; it doesn't matter

2. Hi-Z: High impedance

3. $\overline{\mathbf{Q}}_0$: Q level prior to determination of input condition shown in table







	Paramete	r	Symbol	Rating	Unit	
Supply voltage		Vcc	$-0.5 \sim +7.0$	V		
Input/output voltage		oltage		$-0.5 \sim V_{CC} + 0.5$	V	
Input protect	tion diode current		I _{IК} ±20		mA	
Output paras	sitic diode current		I _{OK} ±20		mA	
Output curre	put current		Ιο	±35	mA	
Supply curre	ent	t		±70	mA	
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$	
	MN74HC536	Ta=-40~+60°C	P_{D}	400	m W	
Power	MIN74HC550	Ta=+60~+85℃	F ()	Decrease to 200mW at the rate of 8mW/°C	m w	
dissipation	pation MN74HC536S Ta=-40		P_{D}	275	mW	
	MN74HC5505	Ta=+60~+85℃	F))	Decrease to 200mW at the rate of 3.8mW/°C	m vv	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

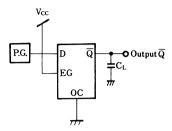
		Vcc	Te	st Condition	ons		Te	mperat	ure		
Parameter	Symbol		Vı	Io		,	Γa = 25 °	С	Ta=-40)~+85℃	Unit
		(V)	• 1	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	VIH.	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{II} ,	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	Vih	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V _{fL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	УıL	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state	r	6.0	$V_I = V$	IH or V	11.			±0.5		±5.0	μΑ
current	Ioz	0.0	V _o =V	$V_0 = V_{CC}$ or GND				1.0.5		1 5.0	μΑ
Quiescent supply current	Icc	6.0	$V_1 = V_0$	cc or GNI	$I_0=0$			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

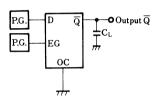
		V_{CC}				mperati			
Parameter	Symbol	(V)	Test Conditions		Ta=25°		Ta=-40	~+85℃	Unit
		(, ,		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			7	15		19	ns
		6.0			ļ	13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				100		125	
$D \rightarrow \overline{Q} (L \rightarrow H)$	t _{PLH}	4.5			12	20		25	ns
		6.0				17		21	
Propagation time		2.0				100		125	
$D \rightarrow \overline{Q} (H \rightarrow L)$	t PHL	4.5			12	20		25	ns
		6.0				17		21	
E Propagation time		2.0				125		155	
Enable $G \rightarrow \overline{Q}(L \rightarrow H)$	t PLH	4.5			15	25		31	ns
2 6 4(2)		6.0				21		26	
E Propagation time		2.0				125		155	
Enable $G \rightarrow \overline{Q}(H \rightarrow L)$	t _{PHL}	4.5			13	25		31	ns
Enable G · Q(II·L)		6.0				21		26	
3-state propagation time		2.0				125		155	
(H→Z)	t _{PHZ}	4.5	$R_L = 1 k\Omega$		14	25		31	ns
(H→Z)		6.0				21		26	
3-state propagation time		2.0				125		155	
(L→Z)	t PLZ	4.5	$R_L = 1 k\Omega$		10	25		31	ns
(L→Z)		6.0				21		26	
3-state propagation time		2.0				100		125	
(Z→H)	t _{PZH}	4.5	$R_L = 1 k\Omega$		9	20		25	ns
(Z→n)		6.0				17		21	
3-state propagation time		2.0				125		155	
(Z→L)	t _{PZL}	4.5	$R_L = 1 k\Omega$		13	25		31	ns
(Z -L)		6.0				21		36	
		2.0				100		125	
Minimum Set-up time	t _{su}	4.5			1	20		25	ns
		6.0				17		21	
		2.0			_	0		0	
Minimum Hold time	th	4.5			_	0		0	ns
		6.0			_	0		0	



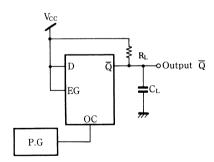
- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , t_{PLH}/t_{PHL} ($D \rightarrow \overline{Q}$)
 - 1. Measuring Circuit (t_{PLH},t_{PHL})



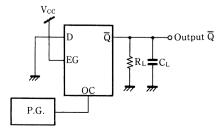
- (2) $t_{PLH}/t_{PHL}(EG \rightarrow \overline{Q})$
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

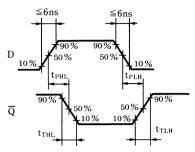


- [3] t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})

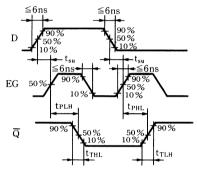


- (4) t_{PLZ}, t_{PZL}
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

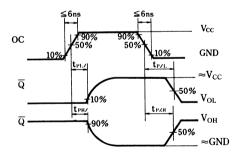




2. Waveforms



2. Waveforms



2. Waveforms

See above [3] 2. for waveforms.

MN74HC564/MN74HC564S

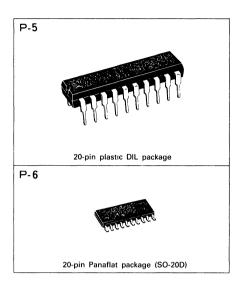
Octal TRI-STATE D-Type Flip-Flops with Inverting Outputs

■ Description

MN74HC564/MN74HC564S contain eight high-speed D-type latches with inverting tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system. D input data satisfying set-up time is inverted and transferred to the output on the positive going edge of clock input.

When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.



■ Truth Table

	Input		Output
Output Control	CLK	D	\overline{Q}
L		L	L
L	5	Н	Н
L	L	×	Q٥
Н	×	×	Hi-Z

Note:

 $1. \ \ \, \int : \quad \, \text{Data input is transferred to output on the positive-going}$

edge from LOW to HIGH of the clock

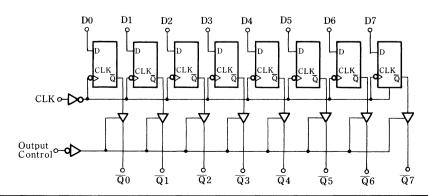
2. ×: Either HIGH or LOW; it doesn't matter

3. Q_O : Q level prior to determination of input condition shown in

table

4. HI-Z: High impedance

Pin Configuration (top view) $20 V_{CC}$ ocl 19 Q 0 D0[2] $18\,ar{ ext{Q}}\,1$ D1 3 $17\bar{\Omega}2$ 16 Q3 D3 5 $\bar{1}\bar{5}\bar{Q}4$ D4 6 $14\,{ar Q}5$ D5 7 13 Ō 6 $12\,ar{Q}7$ D7 9 II CLK GND 10





	Paramete	r	Symbol	Rating	Unit		
Supply voltage	ge			$-0.5\sim+7.0$	V		
Input/output voltage		ltage		ltage		$-0.5 \sim V_{CC} + 0.5$	V
Input protec	tion diode current		I_{1k} ± 20		mA		
Output paras	sitic diode current		Іок	±20	mA		
Output curre	ent	nt		± 35	mA		
Supply curre	ent	t .		±70	mA		
Storage tem	perature range		Tstg	-65~+150	°C		
	MNEANGECA	Ta=-40~+60°C	р	400	111		
Power	MN74HC564	Ta=+60~+85℃	P_{b}	Decrease to 200mW at the rate of 8mW/°C	mW		
dissipation	MN74HC564S	Ta=-40~+60°C	ъ	275	111		
	MIN/4HC5645	Ta=+60~+85℃	\mathbf{P}_{D}	Decrease to 200mW at the rate of 3.8mW/°C	m W		

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V_1, V_0		0~Vcc	V
Operating temperature range	T,		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
•		6.0	0~400	ns

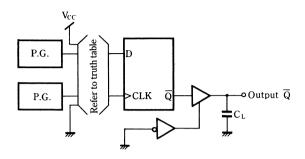
	37		Test Conditions				Te	mperati	ıre		
Parameter	Symbol	V _{CC} (V)	Vı	Io		•	Ta=25 °	3	Ta=-40)~+85℃	Unit
		\ \ \ /	•,		Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2		ļ	4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{II.}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μΑ	4.4	4.5	1	4.4		
Output HIGH voltage	VoH	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VfL	-6.0	mA	3.86			3.76	İ	
		6.0		-7.8	mA	5.36		1	5.26		
		2.0		20.0	μΑ		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VII	6.0	mA	į		0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Iı	6.0	$V_1 = V$	cc or G	ND			±0.1		±1.0	μA
3-state output off state current	Ioz	6.0	$V_1 = V_{1H} \text{ or } V_{1L}$ $V_0 = V_{CC} \text{ or GND}$				±0.5		±5.0	μΑ	
Quiescent supply current	Icc	6.0	$V_1 = V_0$	cc or GNI	$I_0=0$			8.0		80.0	μA

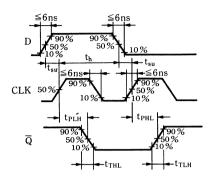
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

		(37)			Te	mperatu	re		
Parameter	Symbol	(V)	Test Conditions		Ta=25°	2	Ta=-40	0~+85℃	Unit
		Vcc		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t TLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t THL	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				125		155	
Propagation time $CLK \rightarrow \overline{Q} (L \rightarrow H)$	t PLH	4.5			16	25		31	ns
CLK→Q (L→H)		6.0				21	ŀ	26	
Duran anation time		2.0				125		155	
Propagation time	t PHL	4.5			14	25		31	ns
$CLK \rightarrow \overline{Q} (H \rightarrow L)$		6.0				21		26	
2 -1-1		2.0				150		190	
3-state propagation time	t PHZ	4.5	$R_L = 1 k\Omega$		15	30		38	ns
$(H \rightarrow Z)$		6.0				26		33	
0		2.0				150		190	
3-state propagation time	t PLZ	4.5	$R_L = 1 k\Omega$		18	30		38	ns
$(L \rightarrow Z)$		6.0				26		33	
3-state propagation time		2.0				125		155	
	t _{PZH}	4.5	$R_L = 1 k\Omega$		13	25		31	ns
(Z→H)		6.0				21		26	
2 state proposetion time		2.0				125		155	
3-state propagation time	t PZI.	4.5	$R_L = 1 k\Omega$		15	25		31	ns
(Z→L)		6.0				21		26	
		2.0				100		125	
Minimum Set-up time	tsu	4.5			1	20		25	ns
-		6.0				17		21	
		2.0			_	0		0	
Minimum Hold time	th	4.5			_	0		0	ns
		6.0			_	0		0	
		2.0		6			4		
Maximum clock frequency	fmax	4.5		30	42		24		MHz
		6.0		35			28	1	

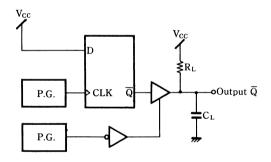


- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , $t_{PLH}/t_{PHL}(CLK \rightarrow \overline{Q})$, t_{su} , t_h , f_{max}
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

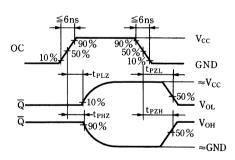




- (2) t_{PHZ} , t_{PZH}
 - 1. Measuring Circuit (t_{PLH},t_{PHL})



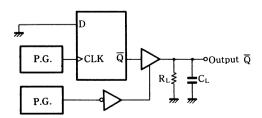
2. Waveforms



- (3) t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

2. Waveforms

See above [2] 2. for waveforms.



20 V_{CC} 19 Q 0 18 Q 1 17 Q2 16 Q3

15 Q 4

14 Q 5

MN74HC573/MN74HC573S

Octal TRI-STATE D-Type Latches

■ Description

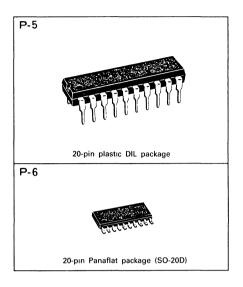
MN74HC537/MN74HC573S contain eight high-speed D-type latches with tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system.

When output disable input is LOW and latch enable input is HIGH, the output outputs the data input state.

When latch enable is LOW, the data input data is held in the output until when latch enable input becomes HIGH.

When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.



Pin Configuration (top view)

■ Truth Table

	Input						
Output Control	G	D	Q				
L	Н	Н	Н				
L	Н	L	L				
L	L	×	Qo				
Н	×	×	Hi-Z				

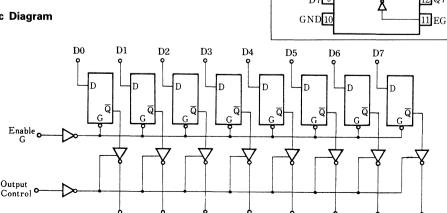
Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance
- 3. Q₀: Q level prior to determination of input condition shown in

Q0

Q1

■ Logic Diagram



Q2

Q3

Q4

Q5

Q6

Q7

	Parameter	-	Symbol	Rating	Unit		
Supply voltag	e		ply voltage		$V_{\rm cc}$	−0.5∼+7.0	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	v		
Input protect	ion diode current		I _{IK}	±20	mA		
Output paras	Output parasitic diode current			±20	mA		
Output current			Io	±35	mA		
Supply curre	nt		Icc, I _{GND}	±70	mA		
Storage temp	perature range		Tstg	-65~+150	°C		
	MN74HC573	Ta=-40~+60℃	P_D	400	337		
Power	T 100 105°0		FD	Decrease to 200mW at the rate of 8mW/°C	mW		
dissipation	issipation MN74HC573S $Ta=-40\sim+60^{\circ}$		D.	275	337		
	$\begin{array}{c c} MN74HC573S & \hline T_a = +60 \sim +85 \% \end{array}$		P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	mW		

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0∼V _{cc}	V
Operating temperature range	T_{A}		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

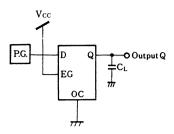
		V_{CC}	Test Conditions			T	emperatu	re			
Parameter	Symbol	(V)	Vı				Ta=25°		Ta=-40	0~+85℃	Unit
		(v)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{1L}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36		l	5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	II	6.0	V _I =	V _{CC} or	GND			±0.1		±1.0	μA
3-state output off state current	Ioz	6.0	$V_{I} = V_{I}$ $V_{O} = V_{O}$	H or V _{IL}	ID			±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GN	D, I ₀ =0			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

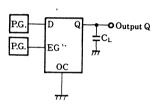
		3.7			Te	mperat	ure		
Parameter	Symbol	Vcc	Test Conditions	-	Γa=25°C		$T_a = -40$	~+85°C	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5			7	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	tTHL	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				100		125	
D \rightarrow Q (L \rightarrow H)	tPLH	4.5			11	20		25	ns
D-7Q (L -11)		6.0				17		21	
Propagation time		2.0				100		125	
D→Q (H→L)	t _{PHL}	4.5			12	20		25	ns
D • Q (II • L)		6.0				17		21	
Propagation time		2.0				125		155	
Enable $G \rightarrow Q(L \rightarrow H)$	t PLH	4.5			15	25		31	ns
Emable (1.44(EII)		6.0				21		26	
Propagation time		2.0				150		190	
Enable G→Q(H→L)	t _{PHI}	4.5			16	30		38	ns
Enable G-Q(n-L)		6.0				26		33	
3-state propagation time		2.0				125		155	
	tPHZ	4.5	$R_L = 1 k \Omega$	1	10	25		31	ns
$(H \rightarrow Z)$		6.0				21		26	
0		2.0				125		155	
3-state propagation time	tPLZ	4.5	$R_L = 1 k \Omega$	1	9	25		31	ns
$(L \rightarrow Z)$		6.0		1		21		26	
3-state propagation time		2.0				100		125	
	tpzn	4.5	$R_L = 1 k \Omega$		9	20		25	ns
(Z→H)		6.0				17		21	
3-state propagation time		2.0				100		125	
	tPZL	4.5	$R_L = 1 k \Omega$		11	20		25	ns
(Z→L)		6.0				17		21	
		2.0				100		125	
Minimum Set-up time	tsu	4.5			2	20		25	ns
		6.0				17		21	
		2.0			_	0		0	
Minimum Hold time	t _h	4.5			-	0		0	ns
		6.0		}	_	0		0	



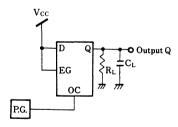
- Switching Time Measuring Circuit and Waveforms
- (1) t_{TLH} , t_{THL} , t_{PLH} / t_{PHL} (D \rightarrow Q), t_{su} , t_h
 - 1. Measuring Circuit (t_{PLH},t_{PHL})



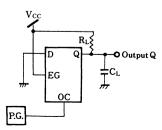
- (2) $t_{PLH}/t_{PHL}(EG \rightarrow Q)$
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

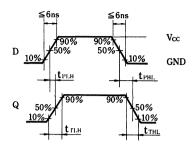


- (3) tphz, tpzh
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})

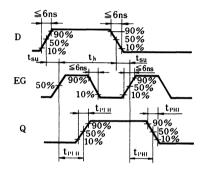


- (4) tPLZ, tPZL
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

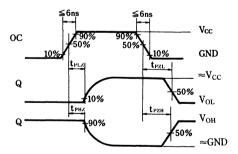




2. Waveforms



2. Waveforms



2. Waveforms

See above [3] 2. for waveforms.

MN74HC574/MN74HC574S

Octal TRI-STATE D-Type Flip-Flops

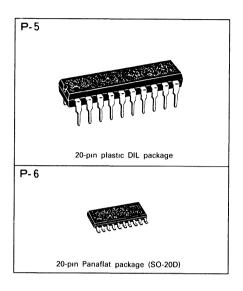
Description

MN74HC574/MN74HC574S contain eight high-speed D-type flipflops with trip-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system.

D input data satisfying set-up time is inverted and transferred to the output on the rising edge of clock input.

When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly drive. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.



■ Truth Table

	Input							
Output Control	CLK	D	Q					
L	£	Н	Н					
L,	5	L	L					
L	L	×	Qo					
Н	×	×	Hi-Z					

Note:

 1.
 √: Data input is transferred to output on the negative-going edge from LOW to HIGH of the clock

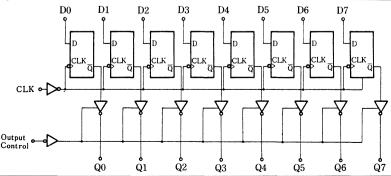
2. ×: Either HIGH or LOW; it doesn't matter

3. Q_O: Q level prior to determination of input condition shown

ın table

4. H₁-Z: High impedance

Pin Configuration (top view) OC 1 D0 2 D Q D1 3 D2 4 D Q D1 3 D2 4 D Q LLK OD D Q 16 Q3 D4 6 D Q CLK OD D Q 18 Q1 17 Q2 D3 5 CLK OD D Q 18 Q1 17 Q2 D3 6 D Q CLK OD D Q 18 Q1 17 Q2 D3 6 D Q CLK OD D Q 18 Q1 17 Q2 D3 6 D Q CLK OD D Q 18 Q1 17 Q2 D3 6 D4 6 D5 7 D6 8 D7 9 CLK OD D Q CLK OD D Q 12 Q7 CLK OD GND 10 CLK OD TICLK



	Parameter		Symbol	Rating	Unit				
Supply voltag	ltage		pply voltage		ply voltage		Vcc	-0.5∼+7.0	V
Input/output	voltage		V _I , V _O	-0.5~V _{CC} +0.5	V				
Input protect	tion diode current		I _{IK}	±20	mA				
Output paras	Output parasitic diode current			±20	mA				
Output curre	Output current		current		Io	±35	mA		
Supply curre	ent	t		±70	mA				
Storage temp	perature range		Tstg	−65∼+150	$^{\circ}$				
	MN74HC574	Ta=-40~+60°C	P_{D}	400	W				
Power	$Ta = +60 \sim +85^{\circ}$		FD	Decrease to 200mW at the rate of 8mW/°C	mW				
dissipation	tion MN74HC574S Ta=−40~+60 ℃		D.	275					
	$T_{a}=+60\sim+85$ °		P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW				

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

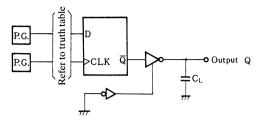
		V_{CC}	Test Conditions			Т	emperati	ure			
Parameter	Symbol	(V)	V.	V _I I _O F			Γa=25℃)	Ta=-40)~+85℃	Unit
		(•)	V1	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V _{IH}	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}	6.0	or	-20.0	μ A	5.9	6.0		5.9		V
		4.5	V_{IL}	-6.0	mA	3.86		İ	3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μΑ		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μ A		0.0	0.1		0.1	V
		4.5	VIL	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Ιı	6.0	$V_1 = V_C$	c or GN	D			±0.1		±1.0	μA
3-state output off state	_		$V_I = V$	in or Vi	L						
current	Ioz	6.0	$V_0 = V_0$	c or GN	D			±0.5		±5.0	μΑ
Quiescent supply current	I _{cc}	6.0	$V_I = V_C$	c or GNI	D, I ₀ =0			8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

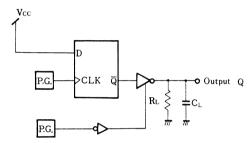
		.,,			Te	mperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions	-	Γa=25°C		$T_a = -40$)~+85℃	Unit
				min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0		j		13		16	
D		2.0				150		190	
Propagation time	tPLH	4.5			14	30		38	ns
$CLK \rightarrow Q (L \rightarrow H)$		6.0				26		33	
Propagation time		2.0				150		190	
	t _{PHL}	4.5			14	30		38	ns
$CLK \rightarrow Q (H \rightarrow L)$		6.0				26		33	
_		2.0				100		125	
3-state propagation time	t _{PHZ}	4.5	$R_L=1 k\Omega$		11	20		25	ns
$(H \rightarrow Z)$		6.0				17		21	
		2.0				125		155	
3-state propagation time	tPLZ	4.5	$R_L=1 k\Omega$		14	25		31	ns
$(L \rightarrow Z)$		6.0	_			21		26	
_		2.0				100		125	
3-state propagation time	t _{PZH}	4.5	$R_L=1 k\Omega$	1	9	20		25	ns
$(Z \rightarrow H)$		6.0				17		21	
		2.0				100		125	
3-state propagation time	tpzL	4.5	$R_L=1 k\Omega$		11	20		25	ns
$(Z \rightarrow L)$		6.0				17		21	
CONTRACTOR OF THE PARTY OF THE		2.0		1		100		125	
Minimum Set-up time	t su	4.5			2	20		25	ns
•		6.0				17	1	21	
		2.0			_	0		0	
Minimum Hold time	t _h	4.5			_	0		0	ns
The state of the s	•••	6.0			_	0		0	ĺ
		2.0		6			4		
Maximum clock frequency	f max	4.5		30	59		24		MHz
		6.0		35	35		28		



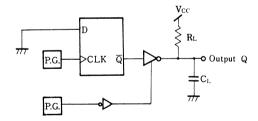
- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , $t_{\text{PLH}}/t_{\text{PHL}}$ (CLKightharpoons Q), t_{su} , f_{max} , t_{h}
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

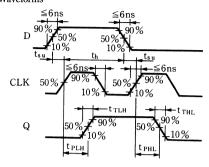


- [2] tphz, tpzh
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

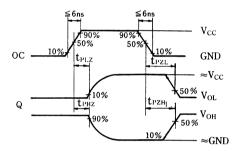


- [3] t_{PLZ}, t_{PZL}
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})





2. Waveforms



2. Waveforms

See above [2] 2. for waveforms.

MN74HC640/MN74HC640S

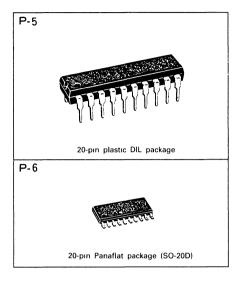
Inverting Octal TRI-STATE Transceivers

■ Description

MN74HC640/MN74HC640S are high speed, inverting bidirectional buffers composed of eight 3-state outputs. Input is transferred bidirectionally, asynchronously through the data bus line. Large current output makes possible high-speed operation for driving a large capacity bus line. It has input G where output becomes enabled at LOW and directional control input DIR.

When DIR input is "H", data is transferred from input A to output B. When DIR input is "L", data is transferred from input B to output A. The transferred data is inverted.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 45LS/74LS logic family.



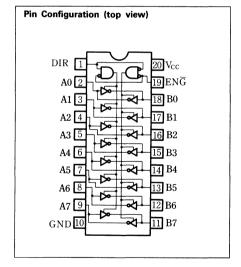
■ Truth Table

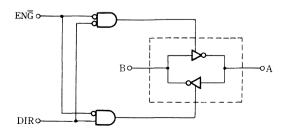
Enable \overline{G}	Direction Control DIR	Operation
L	L	B data to A bus
L	Н	Ā data to B bus
Н	×	Hi-Z

Note:

1. ×: Either HIGH or LOW; it doesn't matter

2. Hi-Z: High impedance







	Parameter			Rating	Unit	
Input/output	ıt/output voltage			-0.5~+7.0	V	
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V	
Input protect	Input protection diode current			±20	mA	
Output parasitic diode current			Іок	±20	mA	
Output current			Io	±35	mA	
Supply curre	Supply current			±70	mA	
Storage temp	perature range		Tstg	-65~+150	$^{\circ}$	
	MN74HC640	Ta=-40~+60°C	P_D	400	mW	
Power	MN/4HC040	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 8mW/°C	mvv	
dissipation	MN74HC640S	$T_{a} = -40 \sim +60 \text{°C}$		275	mW	
	WIW 411C0405	Ta=+60~+85℃	P_{D}	Decrease to 200mW at the rate of 3.8mW/°C	mvv	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	Vcc		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	T _A		-40~+85	°C
		.2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

		V_{CC}	Test Conditions			Temperature					
Parameter	Symbol		Vı	1	,		Ta=25℃			0~+85℃	Unit
		(V)	V I	I _o	Unit	mın.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{II}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	V _{он}	4.5	V _{IH}	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol.	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_1	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
3-state output off state			$V_I = V_{II}$	or VII	,						
current	Ioz	6.0	V _o =V _{cc} or GND		ŀ		±0.5		±5.0	μA	
Quiescent supply current	Icc	6.0	$V_I = V_{C}$	c or GN	D, I ₀ =0			8.0		80.0	μΑ

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

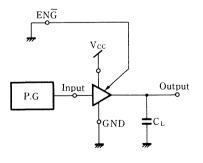
		V_{CC}			Τe	mperat	ure		
Parameter	Symbol		Test Conditions	Ta=25℃			$T_a = -40$	~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5			7	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	tTHL	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				100		125	
(L→H)	t _{PLH}	4.5			10	20		25	ns
(L→H)		6.0				17		21	
Propagation time		2.0				75		95	
• -	tPHL	4.5			9	15		19	ns
$(H \rightarrow L)$		6.0				13		16	
2		2.0				125		155	
3-state propagation time	t PHZ	4.5	$R_L=1 k\Omega$		14	25		31	ns
$(H \rightarrow Z)$		6.0				21		26	
2 -t-t		2.0				150		190	
3-state propagation time	t _{PLZ}	4.5	$R_L=1 k\Omega$		18	30		38	ns
$(L \rightarrow Z)$		6.0				26		33	
		2.0				125		155	
3-state propagation time	t _{PZH}	4.5	$R_L=1 k\Omega$		14	25		31	ns
$(Z \rightarrow H)$		6.0				21		26	
0.14		2.0				125		155	
3-state propagation time	t PZL	4.5	$R_L=1 k\Omega$		15	25		31	ns
$(Z \rightarrow L)$		6.0				21		26	

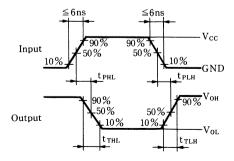
• Switching Time Measuring Circuit and Waveforms

(1) ttlh, tthl, tplh, tphl

1. Measuring Circuit (t_{PLH},t_{PHL})

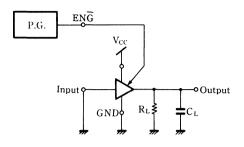
2. Waveforms



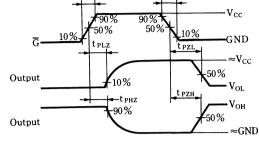




- [2] t_{PHZ}, t_{PZH}
 - 1. Measuring Circuit (t_{PLH},t_{PHL})



- [3] t_{PLZ} , t_{PZL}
 - 1. Measuring Circuit

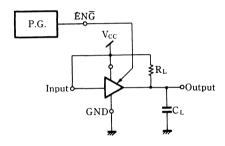


≦6ns

2. Waveforms

2. Waveforms

See above [2] 2. for waveforms.



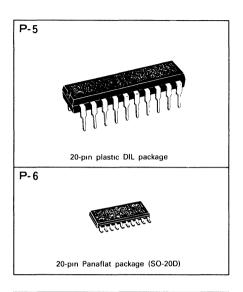
MN74HC643/MN74HC643S

True-Inverting Octal TRI-STATE Transceiver

■ Description

MN74HC643/MN74HC643S are high-speed, true-inverting bidirectional buffers composed of eight 3-state outputs. Input is transferred bidirectionally, asynchronously through the data bus line. Large current output makes possible high-speed operation for driving a large capacity bus line. It has input G where output becomes enabled at LOW and directional control input DIR. When DIR input is "H", data is inverted and transferred from input A to output B. When DIR input is "L", data is transferred from input B to output A.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

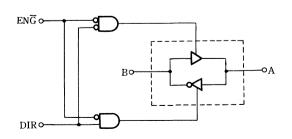


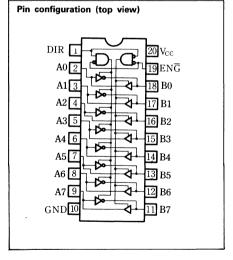
■ Truth Table

Enable G	Direction Control DIR	Operation					
L	L	B data to A bus					
L	Н	A data to B bus					
Н	×	Hi-Z					

Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance







	Parameter		Symbol	Rating	Unit
Supply voltage	oply voltage			-0.5∼+7.0	V
Input/output	voltage		$V_{\rm I}, V_{\rm O}$	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protect	ut protection diode current			±20	mA
Output parasitic diode current			Іок	±20	mA
Output current			Io	±35	mA
Supply curre	Supply current			±70	mA
Storage temp	perature range		Tstg	-65~+150	$^{\circ}$
	MN74HC643	Ta=-40~+60℃	P_{D}	400	mW
Power	WIN7411C045	Ta=+60~+85℃] r _D	Decrease to 200mW at the rate of 8mW/°C	III VV
dissipation	MN74HC643S	Ta=-40~+60℃	D-	275	mW
	MN74HC0435	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	m vv

■ Operating Conditions

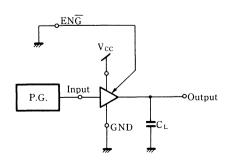
Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

	Vcc	Те	st Conditi	ons	Temperature						
Parameter	Symbol	Symbol	(V) V_{I}	Io r		Ta=25℃			Ta=-40~+85℃		Unit
		(v)	VI	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{II}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
	Vон	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4	ŀ	
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	Vol	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	Ĭι	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
3-state output off state current	Ioz	6.0	V _I =V _{IH} or V _{IL} V ₀ =V _{CC} or GND				±0.5		±5.0	μA	
Quiescent supply current	I _{cc}	6.0	$V_I = V_C$	c or GN	D, $I_0=0$			8.0		80.0	μA

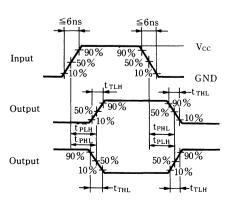
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

		37							
Parameter	Symbol	Vcc	Test Conditions	Ta=25℃			$T_a = -40$	0~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
	:	2.0				75		95	
Output rise time	tтLн	4.5			7	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	tTHL	4.5			6	15		19	ns
		6.0				13		16	
D		2.0				75		95	
Propagation time	t _{PLH}	4.5			8	15		19	ns
(L → H)		6.0				13		16	
Propagation time		2.0				75		95	
(H→L)	t _{PHL}	4.5			8	15		19	ns
(H→L)		6.0				13		16	
3-state propagation time		2.0				125		155	
$(H \rightarrow Z)$	tphz	4.5	$R_L=1_k \Omega$		14	25		31	ns
(H→Z)		6.0				21		26	
2 atata		2.0				125		155	
3-state propagation time	tPLZ	4.5	$R_L=1 K\Omega$		13	25		31	ns
$(L \rightarrow Z)$		6.0				21		26	
0.44		2.0				125		155	
3-state propagation time	t PZH	4.5	$R_L=1 k \Omega$		14	25		31	ns
(Z → H)		6.0				21		26	
		2.0				100		125	
3-state propagation time	tpzl	4.5	$R_L=1 k \Omega$		10	20		25	ns
$(Z \rightarrow L)$		6.0				17		21	

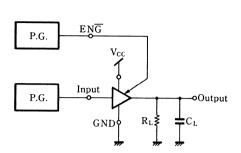
- Switching Time Measuring Circuit and Waveforms
- [1] t_{TLH} , t_{THL} , t_{PLH} , t_{PHL}
 - 1. Measuring Circuit



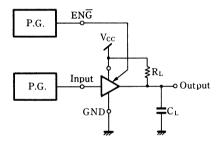
2. Waveforms



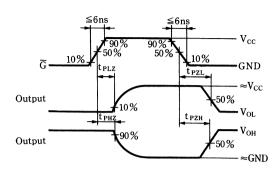
- [2] tphz, tpzh
 - 1. Measuring Circuit



- (3) t_{PLZ}, t_{PZL}
 - 1. Measuring Circuit



2. Waveforms



2. Waveforms

See above [2] 2. for waveforms.

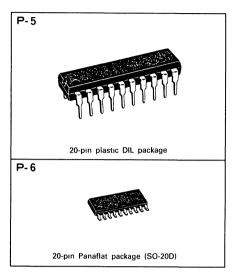
MN74HC688/MN74HC688S

8-Bit Magnitude Comparator (Equality Detector)

■ Description

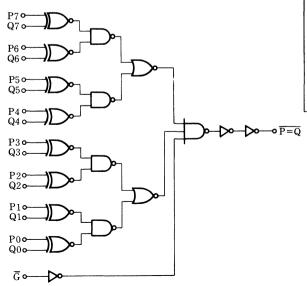
MN74HC688/MH74HC688S are high speed magnitude comparator which compare two eight-bit words and indicate equality, when $\overline{P=Q}$ output is "L", it indicates equality. A single input enabling output at Low level compares words greater than 8 bits, and can be used for easy dependent connection of multiple stages. This circuit can be used for decoding of memory blocks enable signal generated by computer address data.

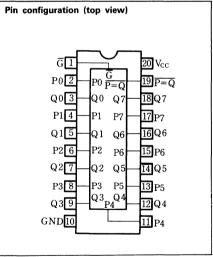
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



■ Truth Table

Inpu	t	
Data	Enable G	P = Q
P, Q	Enable G	
P = Q	L	L
P > Q	L	Н
P < Q	L	Н
×	Н	Н





	Parameter	•	Symbol	Rating	Unit										
Supply voltag	oly voltage		oltage		voltage		ltage		age		$V_{\rm cc}$	-0.5~+7.0	V		
Input/output	Input/output voltage			ut/output voltage			output voltage		voltage		out/output voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protection diode current			I _{IK}	±20	mA										
Output parasitic diode current			Iok	±20	mA										
Output current			I_0	±25	mA										
Supply curre	nt		Icc, IGND	±50	mA										
Storage temp	oerature range		Tstg	-65~+150	င										
	MN74HC688	Ta=-40~+60℃	P_{D}	400	mW										
Power	MN74HC088	Ta=+60~+85 ℃	FD	Decrease to 200mW at the rate of 8mW/°C	m W										
dissipation MN74HC688S		Ta=-40~+60℃	P_{D}	275	mW										
	WIN/4HC0005	Ta=+60~+85℃	l PD	Decrease to 200mW at the rate of 3.8mW/°C	III VV										

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

_ DO GHATACTETISTICS	,		·								
		V_{cc}	Tes	st Condition	ons		Т	emperatu	ıre		
Parameter	Symbol	(V)	V _I	I _o		-	Γa=25°		$T_a = -40$)~+85℃	Unit
		(•)	V I	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage	VoH	6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86		ļ	3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_1	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μΑ
Quiescent supply current	I_{CC}	6.0	$V_I = V_C$	c or GNI	D, I ₀ =0			8.0		80.0	μΑ

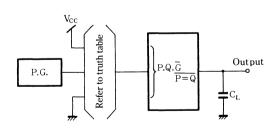
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

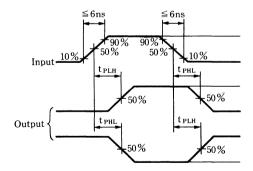
		V			Te	mperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25℃		$T_a = -40$	0~+85℃	Unit
		(*)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	tTHL	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				150		190	
P, $Q \rightarrow P = Q (L \rightarrow H)$	tPLH	4.5			17	30		38	ns
1, Q 1 Q(L II)		6.0				26		33	
Propagation time		2.0				150		190	
• -	tPHL	4.5			14	30		38	ns
$P, Q \rightarrow P = Q (H \rightarrow L)$		6.0				26		33	
Propagation time		2.0				100		125	
$G \rightarrow P = Q (L \rightarrow H)$	tplH	4.5			11	20		25	ns
$G \rightarrow \Gamma = Q (L \rightarrow H)$		6.0				17		21	
D		2.0				100		125	
Propagation time	tpHL	4.5			9	20		25	ns
$G \rightarrow P = Q (H \rightarrow L)$		6.0				17		21	

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit







MN74HC4002/MN74HC4002S

Dual 4-Input NOR Gates

■ Description

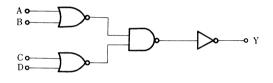
MN74HC4002/MN74HC4002S contain two 4-input positive isolation NOR gate circuits.

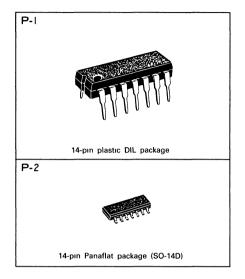
Adoption of a silicon gate CMOS process has made possible a low power dissipation, a high noise margin equivalent to a standard CMOS and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum.

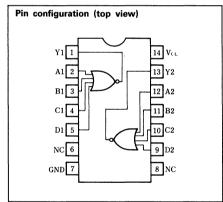
LS TTL 10-inputs can be directly driven.

Resistors and diodes are provided in $V_{\rm CC}$ and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as standard CMOS logic 4000 family.

■ Logic Diagram







■ Absolute Maximum Ratings

	Paramete	r	Symbol	Rating	Unit						
Supply volta	tage		oly voltage		voltage		y voltage		V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_{I}, V_{O}	$-0.5 \sim V_{\rm cc} + 0.5$	V						
Input protection diode current			I _{1K}	±20	mA						
Output parasitic diode current			Іок	±20	mA						
Output current			Ιo	±25	mA						
Supply curre	y current		I_{CC} , I_{GND}	±50	mA						
Storage tem	perature range		Tstg	-65~+150	$^{\circ}$						
	MN74HC4002	Ta=-40~+60°C	ъ	400	117						
Power	MN74HC4002	Ta=+60~+85 ℃	P_D	Decrease to 200mW at the rate of 8mW/°C	mW						
dissipation	MN74HC4002S	Ta=-40~+60°C	D	275	117						
	MN74HC40025	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	mW						

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		1,7	Те	st Conditi	ons		Te	emperatu	re		
Parameter	Symbol	(V)	V			,	Ta=25°	C	Ta=-40)~+85℃	Unit
		(v)	VI	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	VIH	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	VIL	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0	,	-20.0	μA	1.9	2.0		1.9		
	V _{OH}	4.5		-20.0	μ A	4.4	4.5		4.4		
Output HIGH voltage		6.0	VII.	-20.0	μΑ	5.9	6.0		5.9		V
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μΑ		0.0	0.1]	0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μ A		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_I = V_C$	c or GN	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_{\rm I} = V_{\rm Co}$	or GN	$0,I_0=0$			2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

		.,,	-		Te	mperatu	re		
Parameter	Symbol	V _{CC}	Test Conditions		Ta=25°	C	Ta=-40	0~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			6	13		16	
		2.0			25	75		95	
Propagation time	tplH	4.5			8	15		19	ns
(L→H)		6.0			7	13		16	
Decemberation time		2.0			25	75		95	
Propagation time (H→L)	tPHL	4.5			8	15		19	ns
(H→L)		6.0			7	13		16	



MN74HC4015/MN74HC4015S

Dual 4-Stage Shift Registers with Serial-Input/Parallel-Output

■ Description

MN74HC4015/MH74HC4015S contain dual four-stage static shift registers in one chip. Flip-flop at each stage has common clear input, enabling asynchronous clearing with an external input at any time. Flip-flop at each stage is triggered by the rise of the clock pulse.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.

■ Truth Table

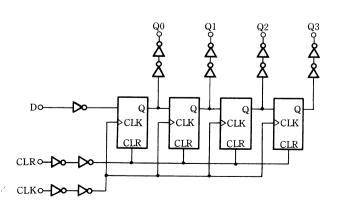
	In	out		Output			
n	CLK	D	CLR	Q_0	Q_1	Q_2	Q_3
1	5	D1	L	D1	×	×	*
2	5	D2	L	D2	D1	×	×
3	5	D3	L	D3	D2	D1	×
4	<i>F</i>	D4	L	D4	D3	D2	D1
	7	×	L		no cl	nange	
	×	×	Н	L	L	L	L

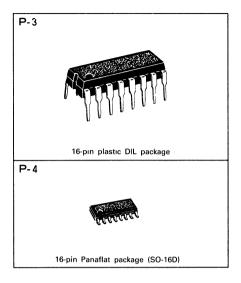
Note:

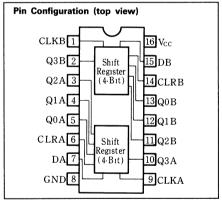
1. ×: Either HIGH or LOW; it doesn't matter

2. D_n: "H" or "L'

3. n: Number of clock pulse
4. T: The rise of clock from "L" to "H"
5. T: The fall of clock from "H" to "L"







	Parameter		Symbol	Rating	Unit			
Input/output	ut/output voltage		V_{CC}	$-0.5 \sim +7.0$	V			
Input/output	Input/output voltage			$-0.5 \sim V_{\rm CC} + 0.5$	V			
Input protect	Input protection diode current			± 20	mA			
Output parasi	Output parasitic diode current			±20	mA			
Output curre	Output current			tput current		Io	±25	mA
Supply curre	t		I _{CC} , I _{GND}	±50	mA			
Storage temp	ge temperature range		Tstg	-65~+150	${\mathbb C}$			
	MN74HC4015	Ta=-40~+60℃	Pp	400	mW			
Power	MN74HC4015	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 8mW/°C	III VV			
dissipation	MN74HC4015S	Ta=-40~+60℃	P_{D}	275	mW			
	MN/47C40155	Ta=+60~+85℃	l rp	Decrease to 200mW at the rate of 3.8mW/°C	111 44			

■ Operating Conditions

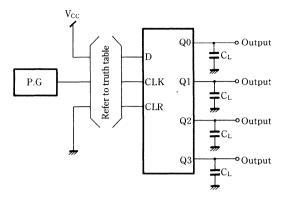
Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0.	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

			Te	st Condition	ons		Т	emperatı	ire		
Parameter	Symbol	V _{CC} (V)	17	_		,	Γa=25°	<u> </u>	Ta=-40	0~+85℃	Unit
		(v)	Vı	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V _{II} .	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OI}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Ιι	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μΑ
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	c or GN	$D, I_0=0$			8.0		80.0	μA

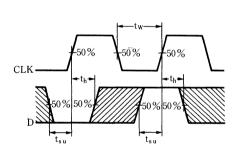
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

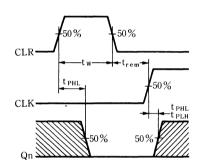
		W			7	`empera	ture		
Parameter	Symbol	V _{CC} (V)	Test Conditions	•	Γa=25°C		$T_a = -40$)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5			10	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	tTHL	4.5			7	15		19	ns
		6.0				13		16	
D :: :		2.0				175		220	
Propagation time	t PLH	4.5			20	35		44	ns
CLK→Qn (L→H)		6.0				30		37	
Propagation time		2.0				175		220	
	t _{PHL}	4.5		ļ	19	35		44	ns
$CLK \rightarrow Q_n (H \rightarrow L)$		6.0				30		37	
D (' ('		2.0				175		220	
Propagation time	tPHL	4.5		ĺ	19	35	}	44	ns
$CLR \rightarrow Qn (H \rightarrow L)$		6.0				30		37	
Minimum pulse width		2.0				125		155	
CLR,CLK	tw	4.5			10	25		31	ns
		6.0				21		26	
		2.0				100		125	
Minimum Set-up time	tsu	4.5		ľ	2	20		25	ns
		6.0				17		21	
		2.0			_	0		0	
Minimum Hold time	th	4.5			_	0		0	ns
		6.0			_	0		0	
		2.0				75		95	
Mınimum recovery time	trem	4.5			7	15		19	ns
		6.0				13		16	
		2.0		6			4		
Maximum clock frequency	fmax	4.5		30	71		24		MHz
nequency		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Cırcuit



2. Waveforms





MN74HC4020/MN74HC4020S

14-Stage Binary Counter

■ Description

MN74HC4020/4020S high-speed 14-Stage binary counter. This counter provides increments on the falling edge of clock input. The clear input operates in the counter, and all outputs $(Q1\sim Q14)$ become "L" regardless of the clock input, when the clear input is "H".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic $4000\,$ family.

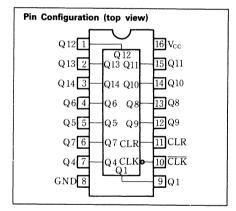
■ Truth Table

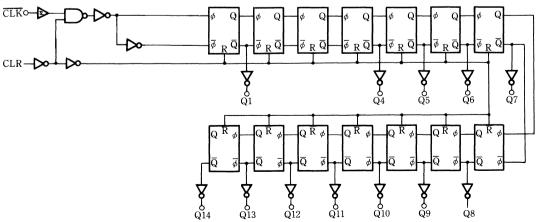
CLK	CLR	Mode
×	Н	All Outputs are low
F	L	No Change
Z	L	Counter Advances

Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. \tag{L}: The fall of clock from "H" to "L"
- 3. ★: The rise of clock from "L" to "H"

P-3 16-pin plastic DIL package P-4 16-pin Panaflat package (SO-16D)





	Parameter		Symbol	Rating	Unit
Supply voltage	Supply voltage			-0.5~+7.0	V
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protect	ion diode current		I _{IK}	±20	mA
Output paras	itic diode current		Ioĸ	±20	mA
Output curre	Output current			±25	mA
Supply curre	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	erature range		Tstg	-65~+150	$^{\circ}$
	MN74HC4020	Ta=-40~+60℃	P_{D}	400	mW
Power	Power $Ta=+60\sim+85^{\circ}$ C		FD	Decrease to 200mW at the rate of 8mW/°C	III VV
dissipation	MN74HC4020S	Ta=-40~+60℃	P_{D}	275	mW
	WIN14HC40205	Ta=+60~+85℃	PD	Decrease to 200mW at the rate of 3.8mW/°C	III VV

■ Operating Conditions

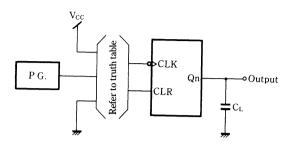
Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm CC}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	T_A		-40~+85	°C.
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

		17	Te	st Conditi	ons		T	`emperatı	ıre		
Parameter	Symbol	Vcc	Vı	Io		•	Γa=25 °C	2	Ta=-40	0~+85℃	Unit
		(V)	*1	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{1L}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μA	1.9	2.0		1.9		
	V _{OH}	4.5	VIH	-20.0	μA	4.4	4.5	ŀ	4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	or GN	$D, I_0=0$			8.0		80.0	μA

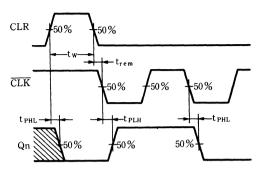
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

		37			Ter	nperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Γa=25°C	;	$T_a = -40$)~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0	·			75		95	
Output fall time	tTHL	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				150		190	
• -	tplH	4.5			16	30		38	ns
$\overline{\text{CLK}} \rightarrow \text{Q1} (L \rightarrow H)$		6.0				26		33	
Propagation time		2.0				150		190	
CLK→Q1 (H→L)	tPHL	4.5			16	30		38	ns
CLK-QI (H-L)		6.0				26		33	
Propagation time		2.0				75		95	
$Q_{n} \rightarrow Q_{n+1} (L \rightarrow H)$	tPLH	4.5			5	15		19	ns
$Qn \rightarrow Qn + I (L \rightarrow II)$		6.0				13		16	
Dana a mationa time a		2.0				75		95	
Propagation time	tPHL	4.5			5	15		19	ns
$Q_{n} \rightarrow Q_{n+1} (H \rightarrow L)$		6.0				13		16	
Propagation time		2.0				150		190	
	tplH	4.5			16	30		38	ns
CLR→Qn (H→L)		6.0				26		33	
Minimum pulse width		2.0				125		155	
CLR	tw	4.5			12	25		31	ns
CLK		6.0				21		26	
		2.0				75		95	
Minimum recovery time	trem	4.5			2	15		19	ns
		6.0				13		16	
Maximum clock		2.0		6			4		
frequency	f max	4.5		30	75		24		MHz
1/		6.0		35			28		

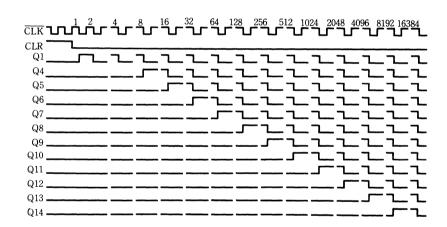
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit



2. Waveforms



■ Typical Operating Conditions



MN74HC4024/MN74HC4024S

7-Stage Binary Counter

■ Description

MN74HC4024/4024S high speed 7-stage ripple-carry counter. This counter provides increments on the falling edge of clock input. The clear input operates in the counter, and all outputs $(Q1\sim Q7)$ become "L" regardless of the clock, when the clear input is "H".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.

■ Truth Table

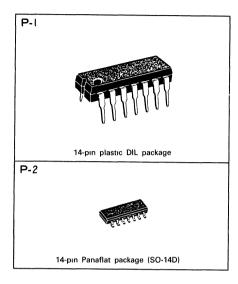
CLK	CLR	Mode
×	Н	All Outputs are low
£	L	No Change
Z	L	Counter Advances

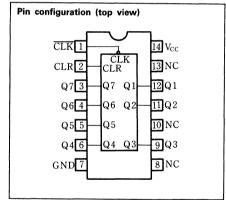
Note:

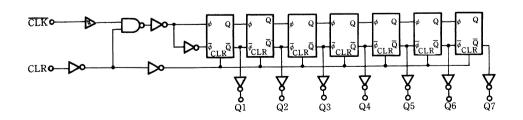
1. ×: Either HIGH or LOW; it doesn't matter

2. \(\cdot\): The fall of clock from "H" to "L"

3. ★: The rise of clock from "L" to "H"







	Parameter		Symbol	Rating	Unit
Supply voltag	Supply voltage			-0.5~+7.0	V
Input/output	voltage		V_{I}, V_{O}	$-0.5 \sim V_{\rm cc} + 0.5$	V
Input protect	ion diode current		I _{IK}	±20	mA
Output paras	itic diode current		Ioĸ	±20	mA
Output curre	Output current			±25	mA
Supply curre	nt		Icc, I _{GND}	±50	mA
Storage temp	oerature range		Tstg	−65~+150	${\mathfrak C}$
	MN74HC4024	Ta=-40~+60℃	P_{D}	400	mW
Power	T 100 105 0			Decrease to 200mW at the rate of 8mW/°C	III VV
dissipation	dissipation MN74HC4024S $Ta=-40\sim+60^{\circ}$			275	mW
	WIN/4HC40245	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	m vv

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	TA		-40~+85	°
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

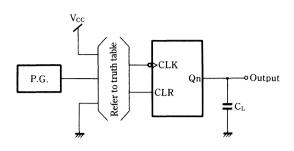
		17	Те	st Condition	ons		Te	emperatu	re		
Parameter	Symbol	Vcc	V_1	Ţ			Γa=25°		Ta=-46	0~+85℃	Unit
		(V)	V ₁	Io	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0	l			4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
	1	6.0		Ì				1.2		1.2	
		2.0	1	-20.0	μA	1.9	2.0		1.9		
	Vон	4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		v
		4.5	VIL	-4.0	mA	3.86		1	3.76		
		6.0	ŀ	-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1	1	0.1	V
		4.5	VIL	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	c or GNI	O, I _o =0			8.0		80.0	μA

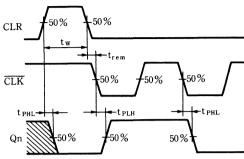
■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

					Tem	peratu	·e		
Parameter	Symbol	Vcc	Test Conditions	-	Γa=25℃		$T_a = -40$)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	tTLH	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	tTHL	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				150		190	
	tplH	4.5			16	30		38	ns
$\overline{\text{CLK}} \rightarrow \text{Q1} (L \rightarrow H)$		6.0				26		33	
Propagation time		2.0				150		190	
	tPHL	4.5			15	30		38	ns
$\overline{\text{CLK}} \rightarrow \text{Q1} (\text{H} \rightarrow \text{L})$		6.0				26		33	
_		2.0				75		95	
Propagation time	t PLH	4.5			5	15		19	ns
$Qn \rightarrow Qn + 1 (L \rightarrow H)$		6.0				13		16	
Propagation time		2.0				75		95	
	tPHL	4.5	,		7	15		19	ns
$Qn \rightarrow Qn+1 \ (H \rightarrow L)$		6.0				13		16	
D		2.0				150		190	
Propagation time	tPHL	4.5			17	30		38	ns
$CLR \rightarrow Qn \ (H \rightarrow L)$		6.0				26		33	
Mr. CID I		2.0				125		155	
Minimum CLR pulse	tw	4.5			7	25		31	ns
width		6.0				21		26	
		2.0				75		95	
Minimum recovery time	trem	4.5			4	15		19	ns
		6.0				13		16	
		2.0		6			4		
Maximum clock frequency	f max	4.5		30	98		24		MH_Z
	IIIIA	6.0		35			28		

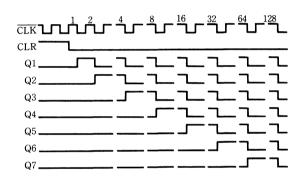
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

2. Waveforms





■ Typical Operating Conditions



MN74HC4040/MN74HC4040S

14-Stage Binary Counter

■ Description

MN74HC4040/4040S high speed12-stage ripple-carry counter. This counter provides increments on the falling edge of clock input. The clear input operates in the counter, and all outputs (Q1~Q12) become "L" regardless of the clock, when the clear input is "H".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.

■ Truth Table

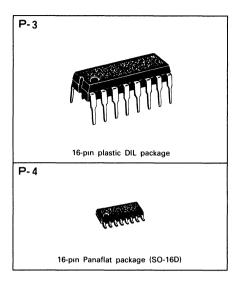
CLK	CLR	Mode
×	Н	All Outputs are low
<i>F</i>	L	No Change
7	L	Counter Advances

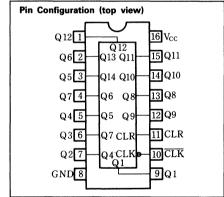
Note:

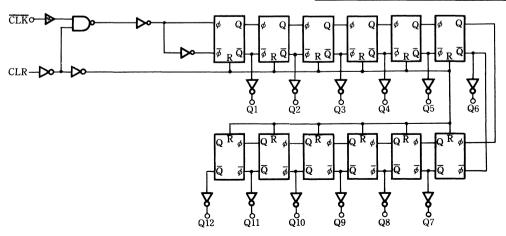
1. ×: Either HIGH or LOW; it doesn't matter

2. \tag{L}: The fall of clock from "H" to "L"

 $3. \mathcal{F}$: The rise of clock from "L" to "H"







	Parameter	-	Symbol	Rating	Unit
Supply voltage	Supply voltage			$-0.5 \sim +7.0$	V
Input/output	voltage		V_{I}, V_{O}	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input protect	tion diode current		I _{IK}	±20	mA
Output paras	sitic diode current		Iok	±20	mA
Output curre	ent		Io	±25	mA
Supply curre	ent		I _{CC} , I _{GND}	±50	mA
Storage tem	perature range		Tstg	-65∼+150	c
	MN74HC4040	Ta=-40~+60℃	P_{D}	400	W
Power	MIN74HC4040	Ta=+60~+85℃	I FD	Decrease to 200mW at the rate of 8mW/°C	mW
dissipation	MN74HC4040S	Ta=-40~+60°C	P_{D}	275	mW
	MIN/4HC40405	Ta=+60~+85°C	l PD	Decrease to 200mW at the rate of 3.8mW/°C	ın vv

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm CC}$		1.4~6.0	V
Input/output voltage	V_{I}, V_{O}		0~V _{cc}	v
Operating temperature range	TA		-40~+85	ဗ
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

			Т	est Condi	tions		Te	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Vı	Io			Γa=25°		Ta=-40)~+85℃	Unit
			V ₁	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5	ļ			3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
	Vон	2.0		-20.0	μA	1.9	2.0		1.9		
		4.5	VIH	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	VIL	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	VIH	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	Iı	6.0	$V_I = V_C$	c or GN	D			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	c or GNI	$I_0=0$			8.0		80.0	μA

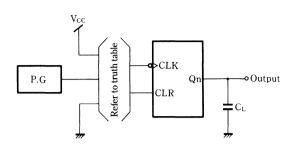


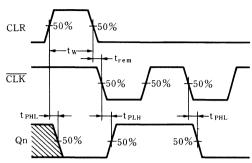
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

					Te	mperat	ure		
Parameter	Symbol	V _{CC} (V)	Test Conditions	7	Γa=25℃	,	$T_a = -40$	0~+85℃	Unit
				min.	typ.	max.	min.	max.	
		2.0			25	75		95	
Output rise time	t _{TLH}	4.5			12	15		19	ns
		6.0			10	13		16	
		2.0			20	75		95	
Output fall time	t _{THL}	4.5			9	15		19	ns
		6.0			8	13		16	
D		2.0			55	200		250	-
Propagation time	tplH	4.5			20	40		50	ns
$\overline{C}\overline{L}\overline{K} \rightarrow Q1 \ (L \rightarrow H)$		6.0			15	34		43	
		2.0			50	175		220	
Propagation time	t _{PHI} .	4.5			18	35		44	ns
CLK→Q1 (H→L)		6.0			15	30		37	
		2.0			18	75		95	
Propagation time	tpl.H	4.5			7	15		19	ns
$Qn \rightarrow Qn + 1 (L \rightarrow H)$		6.0			5	13		16	
D		2.0			17	75		95	
Propagation time	t _{PHL}	4.5			6	15		19	ns
$Qn \rightarrow Qn + 1 (H \rightarrow L)$		6.0			5	13		16	
		2.0			55	150		190	
Propagation time	t _{PH1} .	4.5			17	30		38	ns
CLR→Qn (H→L)		6.0			14	26		33	
		2.0			20	75		95	
Minimum CLR pulse	tw	4.5			6	15		19	ns
width		6.0			5	13		16	
		2.0			5	75		95	
Minimum recovery time	trem	4.5			3	15		19	ns
,		6.0			2	13		16	
		2.0		6	25		4		
Maximum clock frequency	f max	4.5		30	70		24		MHz
		6.0		35	80		28		

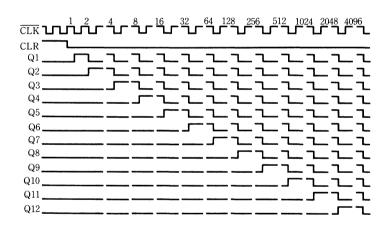
- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH},t_{PHL})

2. Switching Waveforms





■ Typical Operating Condition





MN74HC4049/MN74HC4049S

Hex Inverting Logic Level Down Converters

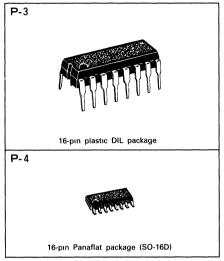
■ Description

MN74HC4049/MN74HC4049S are inverting logic level down converters which function to correct input protection construction. This construction is used for the logic level converter, changing HIGH to LOW logic while it is not operated by LOW logic voltage.

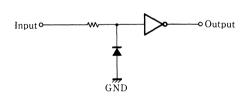
For example, 0-15V CMOS logic can be converted to 0-5V logic when a 5V power supply voltage is used.

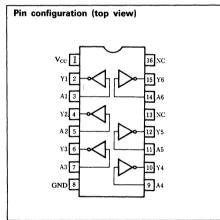
As for corrected input protection, input voltage can exceed the power supply voltage because the diode is not connected to $V_{\rm CC}$. The zener diode connected to GND protects the input against plus-minus quiescent voltage, and can be used as a inverter without level conversion.

Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Same pin configuration and function as the standard CMOS logic 4000 family.



■ Sckematic Diagram





■ Absolute Maximum Ratings

	Paramet	er	Symbol	Rating	Unit
Supply voltage			V _{cc}	-0.5~+7.0	V
Output voltage			Vo	-0.5~V _{CC} +0.5	V
Input voltage			V _I	-0.5~16	V
Input protect	ion diode current		I_{IK}	±20	mA
Output parasi	Output parasitic diode current			±20	mA
Output curre	nt		Io	±35	mA
Supply curren	nt		I _{CC} , I _{GND}	±70	mA
Storage temp	erature range		Tstg	-65~+150	°C
	MN74HC4049	Ta=-40~+60°C	PD	400	mW
Power			1 10	Decrease to 200mW at the rate of 8mW/°C	11144
dissipation $MN74HC4049S$ $Ta=-40\sim+60^{\circ}C$		Ta=-40~+60°C	PD	275	mW
	MIN74HC40495	Ta=+60~+85°C	I ID	Decrease to 200mW at the rate of 3.8mW/°C	11144

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	v
Output voltage	V _O	1	0~V _{CC}	V
Input voltage	V _I		0~15	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	t_r, t_f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

		I	Te	st Condition	ons		Te	mperatur	e		
Parameter	Symbol	V _{CC} (V)	V_1	T .	Io		Ta=25℃)~+85℃	Unit
		` ' '	Vi	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V _{IH}	4.5				3.15			3.15		V
		6.0]		4.2	٠		4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	v
		6.0						1.2	i	1.2	
		2.0		-20.0	μA	1.9	2. 0		1.9		
		4.5		-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	VIL	-20.0	μA	5.9	6.0		5.9		V
		4.5	1	-4.0	mA	3.86			3. 76		
		6.0		-5.2	mA	5. 76			5. 26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5		20.0	μA		0.0	0.1		0.1	
Output LOW voltage	$V_{\rm OL}$	6.0	VIH	20.0	μA		0.0	0.1		0.1	V
•		4.5		4.0	mA			0.32	ł	0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_1	6.0	$V_I = V_{CC}$	or GNI)			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_{\rm I} = V_{\rm C}$	c or GN	$0,I_0=0$			4.0		40.0	μΑ

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

					Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°		Ta=-40)~+85℃	Unit
		(•)		min.	typ.	max.	min.	max.	
		2.0			19	75		95	
Output rise time	tTLH	4.5			10	15		19	ns
		6.0			9	13		16	
		2.0			18	75		95	
Output fall time	t _{THI} .	4.5			10	15		19	ns
		6.0			8	13		16	
ъ.		2.0			15	100		125	
Propagation time (L→H)	tPLH	4.5			11	20		25	ns
(L · II)		6.0			10	17		21	
		2.0			18	100		125	
Propagation time (H→L)	t _{PHL}	4.5			11	20		25	ns
		6.0			9	17		21	



MN74HC4050/MN74HC4050S

Hex Logic Level Down Converter

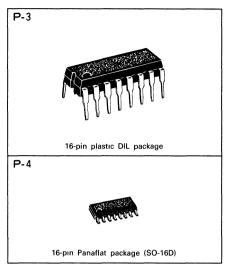
■ Description

MN74HC4050/MN74HC4050S are non-inverted logic level down converts which function to correct input protection construction. This construction is used for the logic level converter, changing HIGH to LOW logic while it is not operated by LOW logic voltage.

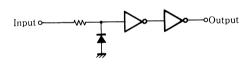
For example, 0-15V CMOS logic can be converted to 0-5V logic when a 5V power supply voltage is used.

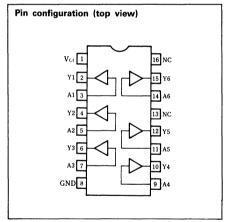
As for corrected input protection, input voltage can exceed the power supply voltage because the diode is not connected to $V_{\rm CC}$. The zener diode connected to GND protects the input against plus-minus quiescent voltage, and can be used as a buffer without level conversion.

Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Same pin configuration and function as the standard CMOS logic 4000 family.



■ Sckematic Diagram





■ Absolute Maximum Ratings

	Paramete	er	Symbol	Rating	Unit	
Supply voltag	e		V _{cc}	-0.5~-7.0	V	
Output voltage			V _o	-0.5~V _{CC} +0.5	V	
Input voltage			V _I	-0.5~16	V	
Input protect	ion diode current		I _{IK}	±20	mA	
Output parasitic diode current			I _{OK}	±20	mA	
Output curre	nt		Io	±35	mA	
Supply curren	nt		I _{CC} , I _{GND}	±70	mA	
Storage temp	erature range		Tstg	-65~+150	°C	
	MAISTICAGEO	Ta=-40~+60°C	PD	400		
Power	MN74HC4050	Ta=+60~+85°C	7 70	Decrease to 200mW at the rate of 8mW/°C	mW	
dissipation	MN74HC4050S	Ta=-40~+60°C	PD	275	mW	
	MIN/4HC40505	Ta=+60~+85°C] PD	Decrease to 200mW at the rate of 3.8mW/°C	mvv	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V _{cc}		1.4~6.0	V
Output voltage	V _o		0~V _{CC}	V
Input voltage	V _I		0~15	V
Operating temperature range	T _A		-40∼+85	°C
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

								mperatu			
:		.,	Tes	st Condition	ons						
Parameter	Symbol	V _{CC} (V)	$V_{\rm I}$	I _O		Ta=25℃			Ta=-40~+85℃		Unit
			V I	10	Unit	min.	typ.	max.	min.	max.	
		2.0				1.5			1.5		
Input HIGH voltage	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
		4.5		-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V _{OH}	6.0	V _{IH}	-20.0	μA	5.9	6.0	ļ	5.9		V
		4.5		-4.0	mA	3.86		İ	3.76		
		6.0		-5.2	mA	5.36			5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5		20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	VIL	20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_{I}	6.0	$V_I = V_{CO}$	c or GN	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CO}$	c or GNI	$D,I_0=0$			4.0		40.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

					Τe	mperatu	re		I Init
Parameter	Symbol	(V)		Ta=-40)~+85℃	Unit			
				min.	tуp.	max.	min.	max.	
		2.0			21	75		95	
Output rise time	tilH	4.5			8	15		19	ns
		6.0			7	13		16	
		2.0			13	75		95	
Output fall time	t _{THL}	4.5			7	15		19	ns
		6.0			5	13		16	
_		2.0			39	75		95	
Propagation time (L→H)	t _{PLH}	4.5			8	15		19	ns
(L -11,		6.0			7	13		16	
Propagation time (H→L)		2.0			10	75		95	
	tPHL	4.5			8	15		19	ns
		6.0			6	13		16	



MN74HC4051/MN74HC4051S

Single 8-Channel Multiplexer/Demultiplexer

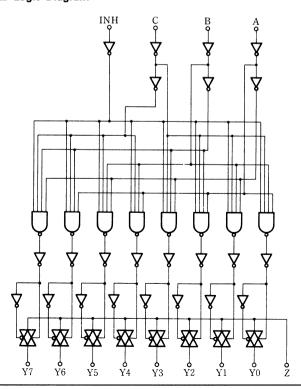
■ Description

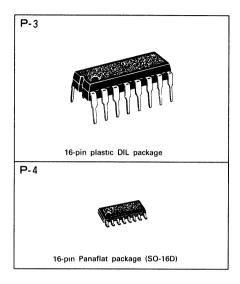
MN74HC4051/MN74HC4051S are an analog multiplexer which controls 8-channel analog switch with three input digital signal. Since each switch ON resitance is low, this chip can be connected to low impedance circuits. Pin configuration is same as the standard CMOS logic 4000 family.

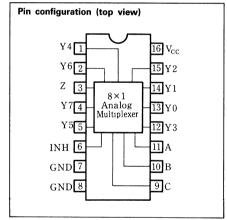
■ Truth Table

	I nput								
INH	С	В	A	ON					
L	L	L	L	Y0 - Z					
L	L	L	Н	Y1-Z					
L	L	Н	L	Y2-Z					
L	L	Н	Н	Y3 – Z					
L	Н	L	L	Y4-Z					
L	Н	L	Н	Y5 – Z					
L	H	Н	L	Y6 – Z					
L	Н	Н	Н	Y7 – Z					
Н	×	×	×	All OFF					

Note: x: don't care







	Paramete	r	Symbol	Rating	Unit			
Supply voltage	ge		V_{CC}	$-0.5\sim+7.0$	V			
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{\rm CC} + 0.5$	V			
Input protection diode current			I _{IK}	±20	mA			
Output parasitic diode current			Іок	±20	mA			
Output current			Io	± 35	mA			
Supply curre	Supply current			ırrent		I _{CC} , I _{GND}	± 70	mA
Storage tem	perature range		Tstg	-65 ∼+150	$^{\circ}$			
	MN74HC4051	Ta=-40~+60°C	P_{D}	400	mW			
Power	MN74HC4051	Ta=+60~+85℃	FD	Decrease to 200mW at the rate of 8mW/°C				
dissipation	dissipation MN74 HC4051 S	Ta=-40~+60°C	D	275	mW			
	WIN74 HC40515	Ta=+60~+85℃	P_D	Decrease to 200mW at the rate of 3.8mW/°C	m vv			

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		2.0~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	TA		-40~+85	°C
		2.0	0~1000	ns
Input rise and fall time	tr, tf	4.5	0~500	ns
		6.0	0~400	ns

		Vcc			Te	mperatu	ıre		
Parameter	Symbol		Test Conditions	-	Γa=25℃		Ta=-40)~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
		2.0		1.5			1.5		V
Input HIGH voltage	VIH	4.5		3. 15]		3. 15		V
		6.0		4. 2			4. 2		V
		2. 0				0.3		0.3	V
Input LOW voltage	VIL	4.5				0.9		0.9	wax. V V V V V 0.3 V 0.9 V 1.2 V ±1.0 μA 80.0 μA
		6.0				1.2		1.2	V
Input current	Ιı	6.0	V _I = V _{CC} or GND			±0.1		±1.0	μA
0	т		V _I =V _{CC} or GND		}	0.0		00.0	μΑ
Quiescent supply current	I_{CC}	6.0	$I_0=0$			8.0		80.0	
Input/output off reak current	I S(off)	6.0	$V_I = V_{IH} \text{ or } V_{IL}$ $ V_S = V_{CC} \text{ or GND}$			±0.1		±1.0	μA
		2.0			1000	2000		3000	Ω
On resistance	D	3.0	W. W. CMD		200	400		600	Ω
On resistance	Ron	4.5	$V_{is} = V_{CC} \sim GND$		80	160		240	V V V V V V μΑ μΑ Ω Ω
		6.0			60	120		130	
		2. 0			150				Ω
Variation of On	AD	3. 0			25				Ω
resistance	ΔR_{ON}	4.5			10				Ω
		6.0			7				Ω



■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

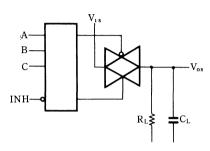
		,,			T	empera	ture			
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25℃			0~+85℃	Unit	
		(v)		min.	typ.	max.	min.	max.	ns ns ns	
D		2.0	$R_L=1 k\Omega$			50		65		
Propagation time	tPHL	4.5	$C_L=50 \mathrm{pF}$			10		13	ns	
$Vis \rightarrow Vos (H \rightarrow L)$		6.0	-			9		11	ns ns	
Dropo mation time		2.0	INH=GND			50		65		
Propagation time Vis→Vos (L→H)	tplH	4.5	Input transition			10		13	ns	
VISTVOS (LTI)		6.0	time = 15 ns			9		11		
Dunan mation time		2.0				150		190		
Propagation time	tPHL	4.5	$R_L = 1 k\Omega$			30		38	ns	
A, B, $C \rightarrow V$ os $(H \rightarrow L)$		6.0	$C_{L} = 50 \text{pF}$			26		33	ns ns ns ns MHz	
Duese action time		2.0	INH=GND			150		190		
Propagation time	tplH	4.5	INH-GND			30		38	ns ns ns ns s s s s s s s s s s s s s s	
$A, B, C \rightarrow V_{OS} (L \rightarrow H)$		6.0				26		33		
		2.0				150		190		
Output Disable Time INH \rightarrow V _{OS} (H)	tphz	4.5				330		38	ns	
		6.0				26		33	ns ns ns ns MHz	
Output Disable Time INH \rightarrow V _{OS} (L)		2.0				150		190		
	tPLZ	4.5	$R_L = 1 k\Omega$			30		38	ns	
		6.0	$C_L = 50 \mathrm{pF}$			26		33		
		2.0	INH=Vcc			150		190		
Output Enable Time INH \rightarrow V _{OS} (H)	tpzh	4.5	I TATE VCC			30		38	ns	
1411-5 (OS (11)		6.0				26		33		
		2.0				150		190		
Output Enable Time INH→V _{OS} (L)	tPZL	4.5			30		38	ns		
		6.0				26		33		
		2.0	$R_L = 10 k\Omega$							
Sine Wave Distortion		4.5	$C_L = 50 \text{ p F}$ $f_i = 1 \text{ kHz}$		0.1				%	
		6.0	$Y = \frac{1}{2}V_{CC}(P-P)$							
		2.0	$R_L = 1 k\Omega$							
Crosstalk 2 channel		4.5	$Y = \frac{1}{2} V_{CC}(P - P)$		t.b.f				MHz	
		6.0	1- 2 VCC(1 1)							
		2.0	$R_L = 10 k\Omega$							
Crosstalk (Address Input→Output)		4.5	$C_L = 50 pF$		t.b.f				m V	
		6.0	INH or A, B, C=Vcc							
Foodthrough		2.0	$R_L = 10k\Omega$							
Feedthrough (OFF)		4.5	$ \begin{array}{l} Y = \frac{1}{2} V_{CC} (P - P) \\ C_L = 50 pF \end{array} $		t.b.f				MHz	
(Off)		6.0	INH=GND							
·		2.0	$R_L = 1 k\Omega$							
Frequency Response		4.5	$ KL - 1 kt^{2} $ $ INH = \frac{1}{2} V_{CC} (P-P)$		t.b.f				MHz	
		6.0	IIVII— 2 V CC (F-F)							

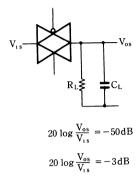
• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit

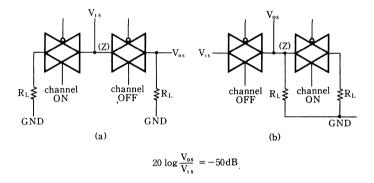
(Fig. 1) Progation Delay Time, Output Disable/ Enable Time, Crosstalk Measuring Circuit

(Fig. 2) Sine Wave Distortion, Feedthrough, Frequency Response Measuring Circuit

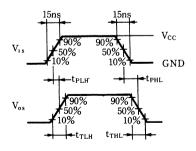


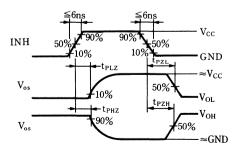


(Fig. 3) Crosstalk Measuring Cirucit



2. Waveforms





MN74HC4052/MN74HC4052S

Dual 4-Channel Analog Multiplexer/Demultiplexer

■ Description

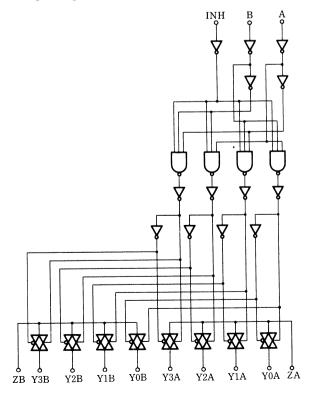
MN74HC4052/MN74HC4052S are dual 4-channel multiplexer/ demultiplexer for analog or digital signals. The switch to each channel become ON with the control signal. Since each switch ON resitance is low, it can be connected to low impedance circuits. Pin configuration is same as standard CMOS logic 4000 family.

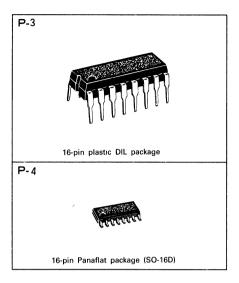
■ Truth Table

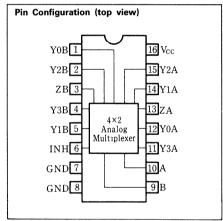
	I nput		Channel ON
INH	В	A	Chainlet ON
L	L	L	Y0A-ZA; Y0B-ZB
L	L	Н	Y1A-ZA; Y1B-ZB
L	Н	L	Y2A-ZA; Y2B-ZB
L	Н	Н	Y3A-ZA; Y3B-ZB
Н	×	×	All OFF

Note:

1. ×: don't care







	Parameter		Symbol	Rating	Unit	
Supply volta	Supply voltage			-0.5~+7.0	V	
Input/output	voltage		V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V	
Input protection diode current			I _{IK}	±20	mA	
Output parasitic diode current			Іок	±20	mA	
Output current			Io	±35	mA	
Supply curre	Supply current			±70	mA	
Storage tem	perature range		Tstg	-65~+150	°C	
	MN74 HC4052	Ta=-40~+60℃	Pn	400	117	
Power	1	Ta=+60~+85℃	l rD	Decrease to 200mW at the rate of 8mW/°C	mW	
dissipation	MN74 HC4052S	Ta=-40~+60℃	P_{D}	275	mW	
	WIN1411C40323	Ta=+60~+85℃	Pb	Decrease to 200mW at the rate of 3.8mW/°C	m vv	

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		2.0~6.0	V
Input/output voltage	V _I , V _O		0~V _{cc}	V
Operating temperature range	TA		-40~+85	r
		2.0	0~1000	ns
Input rise and fall time	t _r , t _f	4.5	0~500	ns
		6.0	0~400	ns

					Te	mperati	ıre		Unit V V V V V μ Α μ Α Ω Ω Ω Ω
Parameter	Symbol	(V)	Test Conditions		Γa= 25°		Ta=-40)~+85°C	
		(*)		min.	typ.	max.	min.	max.	
		2.0		1.5			1.5		V
Input HIGH voltage	VIH	4.5		3. 15	1		3. 15		V
		6.0		4. 2			4. 2		V
		2.0				0.3		0.3	V
Input LOW voltage	V_{1L}	4.5				0.9		0. 9	V
		6.0				1.2		1.2	V
Input current	Ιı	6.0	V _I = V _{CC} or GND			±0.1		±1.0	μA
Quiescent supply current		C 0	$V_I = V_{CC}$ or GND			0.0		80. 0	μA
Quiescent supply current	I cc	6.0	$I_0=0$	i		8.0		80.0	
Input/output off reak	tTHL	6.0	$V_I = V_{IH} \text{ or } V_{IL}$			±0.1		±1.0	μA
current	- 1 1 1 1		Vs = Vcc or GND						
		2.0			1000	2000		3000	
On resistance	Ron	3.0	Vis: Vcc~GND		200	400		600	Ω
On resistance	NON	4.5	VIS. VCC GIVD		80	160		240	V V V V V V μA μA Ω Ω
		6.0			60	120		180	Ω
		2.0			150				Ω
Variation of On	AD	3.0			25				Ω
resistance	ΔR_{ON}	4.5			10				Ω
		6.0			7				Ω

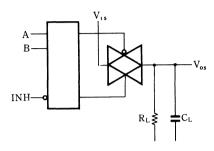
■ AC Characteristics (GND=0V, Input transition time ≤6ns, C_L=50pF)

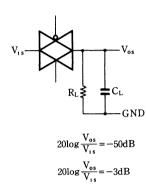
					Ter	nperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25℃		$T_a = -4$	0~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
Propagation time		2.0	$R_L = 1 k\Omega$			50		65	
V _{is} →V _{os} (H→L)	tphL	4.5	$C_L = 50 \text{pF}$			10		13	ns
		6.0	INH= GND			9		11	
Propagation time		2.0				50		65	
Propagation time V _{is} →V _{os} (L→H)	tplH	4.5	Input transition			10		13	ns
15 100 (= 1		6.0	time=15ns			9		11	
D		2.0				150		190	
Propagation time A, B, \rightarrow Vos (H \rightarrow L)	tPHL	4.5	$R_L=1 k\Omega$			30		38	ns
A, B, \rightarrow Vos(H \rightarrow L)		6.0	$C_L = 50 pF$			26		33	ns
		2.0	INH=GND			150		190	
Propagation time	tPLH	4.5	INII—GND			30		38	ns
A, B, \rightarrow Vos(L \rightarrow H)		6.0				26		33	ns ns ns ns ns ns ns
•		2.0				150		190	
Output Disable Time INH \rightarrow V _{OS} (H) tphz	4.5				30		38	ns	
	1 112	6.0				26		33	
		2.0	1		1	150		190	
Output Disable Time INH \rightarrow V _{OS} (L)	tPLZ	4.5				30		38	ns
		6.0	$R_L = 1 k \Omega$			26		33	
Output Enable Time		2.0	$C_L = 50 pF$		-	150		190	
	tpzH	4.5	INH=V _{CC}			30		38	ns
$INH \rightarrow V_{OS}(H)$	"	6.0				26		33	115
		2.0	+		 	150	 	190	
Output Enable Time	tpzl	4.5				30		38	nc
$INH \rightarrow V_{OS}(L)$	L ZL	6.0				26		33	113
		2.0	$R_L=10 k\Omega$		+	20		33	
Sine Wave Distortion		4.5	$C_L = 50 p F$		0.1				ne
		6.0	$f_{i}=1 \text{ H }, Y=\frac{1}{2}V_{CC}(P-P)$		0.1				115
	-	2.0	11 11 11 , 1- 2 VCC(1-F)	-	+			 	
Crosstalk		4.5	$R_L=1 k\Omega$						0/
2 channel		i	$Y = \frac{1}{2} V_{CC} (P - P)$		t.b.f				%
		6.0	D -1010		1		<u> </u>		
Crosstalk		2.0	$R_L = 10k\Omega$						
(Address Input→Output)		4.5	$C_L=50pF$		t.b.f				ns %
	-	6.0	INH or A, B, C=Vcc		ļ			ļ ļ	
Feedthough		2.0	$R_L=10k\Omega$						
(OFF)		4.5	$C_L = 50 p F$	1	t.b.f				MH z
	-	6.0	$INH = GND, Y = \frac{1}{2} V_{CC}(P-P)$				-		
Frequency Response		2.0	$R_L = 1 k\Omega$						
		4.5	$INH = \frac{1}{2} V_{CC}(P-P)$		t.b.f				MHz
		6.0	1111-2 100(1 1)			1	 		

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

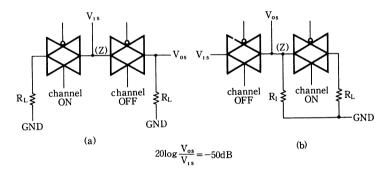
(Fig. 1) Propagation Delay Time, Output Disable/ Enable Time, Crosstalk Measuring Circuit

(Fig. 2) Sine Wave Distortion, Feedthrough, Frequency Response Measuring Circuit

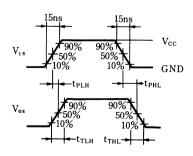


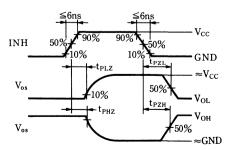


(Fig. 3) Crosstalk Measuring Cirucit



2. Waveforms





MN74HC4053/MN74HC4053S

Triple 2-Channel Analog Multiplexer/Demultiplexer

■ Description

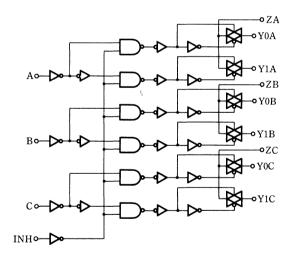
MN74HC4053/MN74HC4053S are triple 2-channel multiplexers/demultiplexers for analog or digital signals. The switch to each channel becomes ON with the control signal. Since each switch ON resitance is low, it can be connected to low impedance circuits. Pin configuration is same as standard CMOS logic 4000 family.

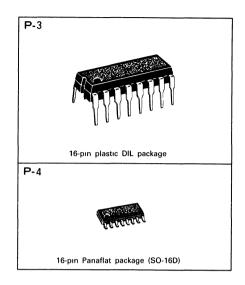
■ Truth Table

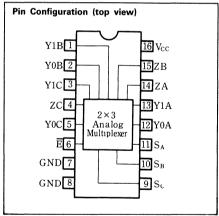
Inpi	ıt	Channel ON
INH	SA	Chamier ON
L	L	Y0A-ZA
L	Н	Y1A-ZA
Н	×	All OFF

Note:

1. ×: don't care







Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	-0.5~+7.0	V
Input/output voltage			V _I , V _O	$-0.5 \sim V_{CC} + 0.5$	V
Input protection diode current			I _{1K}	±20	mA
Output parasitic diode current			Iok	±20	mA
Output current			Io	± 35	mA
Supply current			I _{CC} , I _{GND}	±70	mA
Storage temperature range			Tstg	-65~+150	${}^{\mathbb{C}}$
Power dissipation	MN74 HC4053	Ta=-40~+60℃	P_D	400	mW
		Ta=+60~+85℃	I D	Decrease to 200mW at the rate of 8mW/°C	111 VV
	MNZALICAGESC	Ta=-40~+60℃	P_{D}	275	mW
	MN74HC4053S	Ta=+60~+85℃	r _D	Decrease to 200mW at the rate of 3.8mW/°C	m W

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operating supply voltage	$V_{\rm cc}$		2.0~6.0	V
Input/output voltage	V _I , V _O		$0 \sim V_{CC}$	V
Operating temperature range	TA		-40~+85	°C
	t _r , t _f	2.0	0~1000	ns
Input rise and fall time		4.5	0~500	ns
		6.0	0~400	ns

	Symbol	V _{cc} (V)	Test Conditions	Temperature					
Parameter				Ta=25℃			Ta=-40~+85℃		Unit
				mın.	typ.	max.	min.	max.	
	Vih	2.0		1.5			1.5		V
Input HIGH voltage		4.5		3. 15			3. 15		V
		6.0		4. 2			4. 2		V
	VII	2. 0				0.3		0.3	V
Input LOW voltage		4.5		ļ		0.9		0.9	V
		6.0				1.2		1.2	V
Input current	Ιı	6.0	V ₁ =V _{CC} or GND			±0.1		±1.0	μA
Owen and apply appropri	t I'cc	6.0	V _I =V _{CC} or GND			8.0		90.0	^
Quiescent supply current			$I_0 = 0$					80.0	μΑ
Input/output off reak	Is(off)	6.0	V _I =V _{IH} or V _{IL} V _S =V _{CC} or GND			±0.1		±1.0	μΑ
		2.0		-	1000	2000		3000	Ω
	Ron	3. 0	Vis: Vcc~GND		200	400		600	Ω
On resistance		4.5			80	160		240	Ω
		6.0			60	120		180	Ω
		2.0			150				Ω
		3.0			25				Ω
Variation of On resistance	ΔR_{ON}	4.5			10				Ω
		6.0			7				Ω
		0.0							



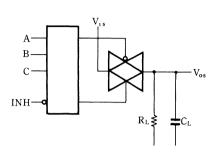
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L =50pF)

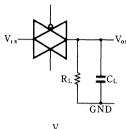
					-	[empera	ture		
Parameter	Symbol	V _{CC} (V)	Test Conditions	,	Ta=25℃	;	Ta=-4	0~+85℃	Unit
		(V)		min.	typ.	max.	min.	max.	
D		2.0	$R_L = 1 k\Omega$			50		65	
Propagation time $V_{is} \rightarrow V_{OS} (H \rightarrow L)$	tphi.	4.5	$C_L = 50 \mathrm{pF}$		5	10		13	ns
Vis VOS (II · L)		6.0	INH= GND			9		11	
D		2.0				50		65	
Propagation time V _{is} →V _{os} (L→H)	tplH	4.5	Input transition		4	10		13	ns
115 105 (2 ==)		6.0	time=15ns			9		11	
D		2.0				150		190	
Propagation time A, B, \rightarrow V _{OS} (H \rightarrow L)	t _{PHL}	4.5	$R_L = 1 k\Omega$		17	30		38	ns
n, b, vos(n · L)		6.0	$C_L = 50 pF$			26		33	
		2.0	INH= GND			150		190	
Propagation time	tplH	4.5	INIT— GND		14	30		38	ns
A, B, \rightarrow Vos(L \rightarrow H)		6.0				26		33	
_		2.0				150	 	190	
Output Disable Time INH→V _{OS} (H)	tpHZ	4.5			18	30		38	ns
2.12. 105 (22)		6.0				26		33	
		2.0	1			150		190	
Output Enable Time INH \rightarrow V _{OS} (L)	tPLZ	4.5			15	30		38	ns
		6.0	$R_L=1 k\Omega$		1	26		33	
	1	2.0	C _L =50pF			150		190	
Output Enable Time		4.5	INH=Vcc		14	30		38	ns
$INH \rightarrow V_{OS}(H)$		6.0				26		33	
		2.0	-		†	150	<u> </u>	190	
Output Disable Time		4.5		15	30		38	ns	
$INH \rightarrow V_{OS}(L)$		6.0			26		33	5	
***************************************		2.0	$R_L = 10 \text{ k}\Omega$			-		00	
Sine Wave Distortion		4.5	$C_L = 50 pF$		0.1			.	%
		6.0	$f_{i}=1 \text{ kHz}, Y=\frac{1}{2} \text{ V}_{CC}(P-P)$		0.1		1		70
		2.0	-1, - 2 (00(11)					 	
Crosstalk		4.5	$R_L = 1 k\Omega$		t.b.f				MHz
2 channel		6.0	$Y = \frac{1}{2} V_{CC} (P - P)$		1.0.1				MITIZ
		2.0	$R_L = 10 k\Omega$		+		 		
Crosstalk		4.5	$C_L = 50 \mathrm{pF}$		t.b.f				mV
$(Address\ Input \rightarrow Output)$		6.0	INH or A, B, C=Vcc		1.0.1				mV
	 	2.0	$R_1 = 10 \text{ k}\Omega$		 		 	 	
Feedthrough		4.5	$C_L = 50 pF$		+ h f				MHz
(OFF)		6.0	$INH = GND,$ $Y = \frac{1}{2} V_{CC}(P-P)$	t.b.f				MHZ	
	-	2.0	1 2 VCC(1 1/				-		
Fraguency Peanonce		4.5	$R_1 = 1 k\Omega$						
Frequency Response	1	6.0	$INH = \frac{1}{2} V_{CC}(P-P)$		t.b.f				MHz
		0.0				<u> </u>			

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit

(Fig. 1) Propagation Delay Time, Output Disadle /Enable Time, Crosstalk Measuring Circuit

(Fig. 2) Sine Wave Distortion, Feedthrough, Frequency Response Measuring Circuit

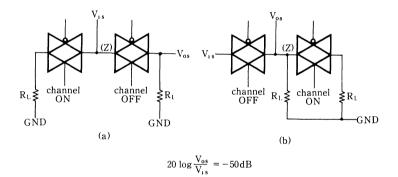




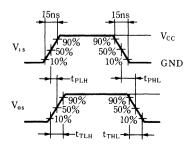
$$20\log\frac{V_{os}}{V_{is}} = -50dB$$

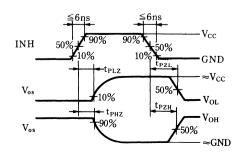
$$20\log\frac{V_{os}}{V_{1s}} = -3dB$$

(Fig. 3) Crosstalk Measuring Cirucit



2. Waveforms







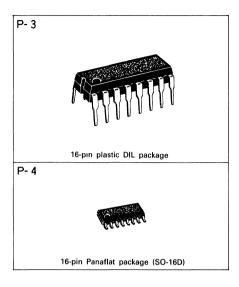
MN74HC4060/MN74HC4060S

14-Stage Ripple-Carry Binary Counter

■ Description

MN74HC4060/4060S are high-speed 14-stage ripple-carry counter. This counter provides increments on the falling edge of clock input. The clear input operates in the counter, and all outputs become "L" regardless of the clock, when the clear input is "H". The clock line is provided with 2-input terminal, which makes the connection with RC or crystal oscillation easy.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 familiy.



16] Vرر

15 Q10

141Q8

13 Q9

12 RESET

10 CLK1 •

9 CLK2

III CLK

Pin Configuration (top view)

Q13

Q14

Q6

Q5

Q7

Q12

CLK2

Q10

Q8

Q9

CLK

CLK1

RESET

Q12 [

Q13[2

Q14[3

Q6 4

Q5 [5

Q7 [6

Q4 [7

GND 8

■ Truth Table

Clock	Reset	Output State
	L	No Change
7	L	Advance to next state
×	Н	All outputs are Low

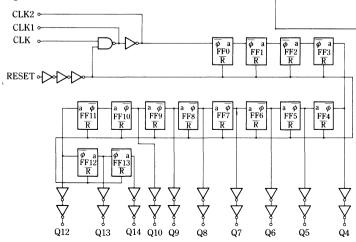
Note:

1. 1: The rise of clock from "L" to "H"

2.\(\tau:\) The fall of clock from "H" to "L"

3. × : Don't care.

■ Logic Diagram



■ Absolute Maximum Ratings

	Paramete	er	Symbol	Rating	Unit
Supply voltage			V _{CC}	-0.5~+7.0	V
Input/output voltage			V _I , V _O	-0.5~V _{CC} +0.5	V
Input protection diode current			I _{IK}	±20	mA
Output parasitic diode current			I _{OK}	±20	mA
Output current			Io	I _O ±25	
Supply curre	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	erature range		Tstg	−65~+150	°C
	MN74HC4060	Ta=-40~+60°C	P _D	.400	mW
Power	WIN7411C4000	$Ta = +60 \sim +85^{\circ}C$	1 D	Decrease to 200m Watt the rate of 8mW/°C	11144
dissipation	MN74HC4060S	Ta+-40~+60°C	D	275	mW
	WIN7411C40003	Ta=+60~+85°C	P _D	Decrease to 200m Watt the rate of 3.8mW/°C	11144

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operation supply voltage	V _{cc}	1	1.4~6.0	V
Input/output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature range	T _A		-40~+85	°C
		2.0	0~1000	
Input rise and fall time	t_r , t_f	4.5	0~500	ns
		6.0	0~400	

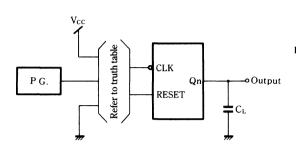
			Tes	t Condition	ons		T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	V	V I		Ta=25°C			$Ta = -40 \sim +85^{\circ}C$		Unit
		(,,	V_1	I_{O}	Unit	mın.	typ.	max.	min.	max.	
Input HIGH voltage		2.0				1.5			1.5		
	V_{IH}	4.5				3.15			3.15		V
		6.0				4.2			4.2		
		2.0						0.3		0.3	
Input LOW voltage	V_{IL}	4.5						0.9		0.9	V
		6.0						1.2		1.2	
		2.0		-20.0	μΑ	1.9	2.0		1.9		
	V _{OH}	4.5	V_{IH}	-20.0	μΑ	4.4	4.5		4.4		
Output HIGH voltage		6.0	or	-20.0	μΑ	5.9	6.0		5.9		V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36		3	5.26		
		2.0		20.0	μA		0.0	0.1		0.1	
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}	6.0	or	20.0	μΑ		0.0	0.1		0.1	V
		4.5	V _{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I _I	6.0	V _I =	V _{CC} or G	ND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$VI = V_{CC}$	or GND	$I_0=0$			8.0		80.0	μA



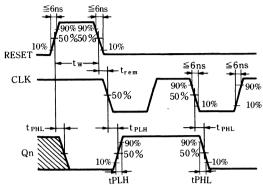
■ AC Characteristics (GND=0V, Input transistion tiem ≤6ns, C_L=50pF)

					Т.	emperatu	re		_
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta = -40	~+85°C	Unit
				min.	typ.	max.	min.	max.	
		2.0				75		95	
Output rise time	t _{TLH}	4.5			8	15		19	ns
		6.0				13		16	
		2.0				75		95	
Output fall time	t _{THL}	4.5			6	15		19	ns
		6.0				13		16	
Propagation time		2.0				330		415	
CLK→Q4	t _{PLH}	4.5				66		83	ns
(L→H)		6.0				56		70	
Propagation time		2.0				330		415	
CLK→Q4 (H→L)	t _{PHL}	4.5				66		83	ns
		6.0				56		70	
Propagation time		2.0				100		125	
$Qn \rightarrow Qn + 1$	t _{PLH}	4.5				20		25	ns
(L→H)		6.0				17		21	
Propagation time	t _{PHL}	2.0				100		125	
$Qn \rightarrow Qn + 1$		4.5				20		25	ns
(H→L)		6.0				17		21	
Propagation time		2.0				150		190	
RESET→Qn	t _{PHL}	4.5				30		38	ns
(H→L)		6.0				26		33	
		2.0				100		125	
Propagation time CLK, RESET	tw	4.5				20		25	ns
		6.0			l	17		21	
		2.0				75		95	
Minimum recovery time	t _{rem}	4.5			l	15		19	ns
		6.0				13		16	
3.6		2.0		6			4		
Maximum clock frequency	f _{max}	4.5		30			24		MHz
rrequency		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms
 - 1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Switching Waveforms





MN74HCT4060/MN74HCT4060S

14-Stage Ripple-Carry Binary Counter (TTL Input)

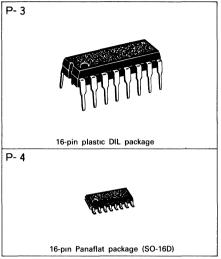
■ Description

MN74HCT4060/MN74HCT4060S are high-speed 14-stage ripplecarry counter. This counter provides increments on the negative going edge of clock input. The clear input operates in the counter, and all outputs become "L" regardless of the clock, when the clear input is "H".

The clock line is provided with 2-input terminal, which makes the connection with RC or crystal oscillation easy.

All inputs are compatible with TTL logic level:0.8V or less is logic "0" input and 2.0V or more is logic "1".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in $V_{\rm CC}$ and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 famility.



■ Truth Table

Clock	Reset	Output State
<u></u>	L	No Change
7	L	Advance to next state
×	Н	All outputs are Low

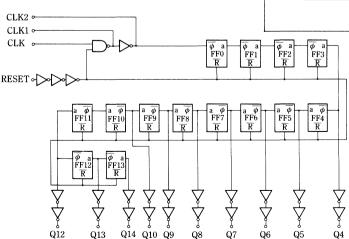
Note:

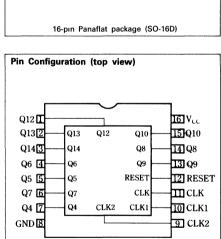
1. 1: The rise of clock from "L" to "H"

2.\(\tau\): The fall of clock from "H" to "L"

3. × : Don't care.

■ Logic Diagram





■ Absolute Maximum Ratings

	Paramete	er	Symbol	Rating	Unit
Supply voltage			V _{cc}	−0.5~+7.0	V
Input/output voltage			V _I , V _O	-0.5~V _{CC} +0.5	- V
Input protecti	ion diode current		I _{IK}	±20	mA
Output parasi	Output parasitic diode current			±20	mA
Output curre	Output current			I _O ±25	
Supply curren	nt		I _{CC} , I _{GND}	±50	mA
Storage temp	erature range		Tstg	−65~+150	°C
	MN74HCT4060	Ta=-40~±60°C	P_{D}	400	mW
Power	WIN74TIC 14000	Ta=+60~+85°C] ID	Decrease to 200m Watt the rate of 8mW/°C	11144
dissipation	MN74HCT4060S	Ta+-40~+60°C	P_{D}	275	mW
	WIN74HC140005	Ta=+60~+85°C	I I	Decrease to 200m Watt the rate of 3.8mW/°C	11144

■ Operating Conditions

Parameter	Symbol	V _{CC} (V)	Rating	Unit
Operation supply voltage	V _{CC}		4.5~5.5	V
Input/output voltage	V _I , V _O		0~V _{CC}	v
Operating temperature range	T _A		-40~+85	°C
Input rise and fall time	t _r , t _f	4.5 .	0~500	ns

			Tes	t Condition	ons		Т	emperatu	re		
Parameter	Symbol	V _{CC} (V)	$V_{\rm I}$	Io			Ta=25°C		Ta=-40	~+85°C	Unit
		(1)	V1	10	Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage		4.5									
	V_{IH}	≀				2.0			2.0		V
		5.5									
		4.5									
Input LOW voltage	V_{IL}							0.8		0.8	V
		5.5									
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
Output HIGH voltage	V_{OH}		or								V
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
Output LOW voltage	V_{OL}		or								V
		4.5	V_{IL}	4.0	mA			0.32		0.37	
Input current	I _I	5.5	V _I =	V _{CC} or G	ND			±0.1		+1.0	μA
Quiescent supply current	I_{CC}	5.5	$V_I = V_{CC}$	or GND	$I_{O}=0$			8.0		80.0	μA

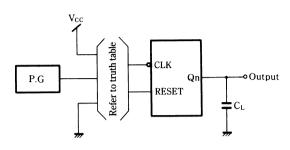


■ AC Characteristics (GND=0V, Input transistion tiem \leq 6ns, C_L =50pF)

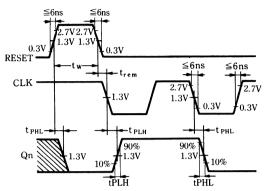
		.,			T	emperatu	re		
Parameter	Symbol	V _{CC} (V)	Test Conditions		Ta=25°C		Ta = -40	~+85°C	Unit
		(,,		min.	typ.	max.	min.	max.	
Output rise time	t _{TLH}	4.5			8	15		19	ns
Output fall time	t _{THL}	4.5			6	15		19	ns
Propagation time $CLK \rightarrow Q4$ $(L \rightarrow H)$	t _{PLH}	4.5				66		83	ns
Propagation time CLK→Q4 (H→L)	t _{PHL}	4.5				66		83	ns
Propagation time $Qn \rightarrow Qn+1$ $(L \rightarrow H)$	t _{PLH}	4.5				20		25	ns
Propagation time $Qn \rightarrow Qn+1$ $(H \rightarrow L)$	t _{PHL}	4.5				20		25	ns
Propagation time RESET \rightarrow Qn (H \rightarrow L)	t _{PHL}	4.5				30		38	ns
Minimum pulse width	t _w	4.5				20		25	ns
Minimum recovery time	t _{rem}	4.5				15		19	ns
Maximum clock frequency	f _{max}	4.5		30			24		MHz

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- Switching Time Measuring Circuit and Waveforms
  - 1. Measuring Circuit (t<sub>PLH</sub>,t<sub>PHL</sub>)



### 2. Switching Waveforms





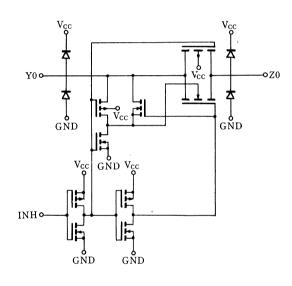
# MN74HC4066/MN74HC4066S

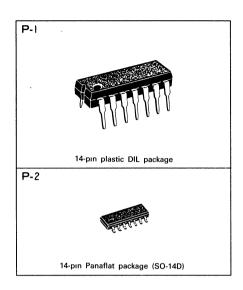
Quad Analog Switch

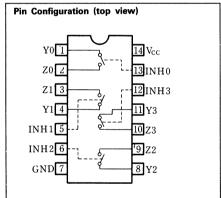
### ■ Description

MN74HC4006/MN74HC4066S are quad independant bidirectional analog switch. When inhibit input (INH) is "H", the state between switch input and output becomes LOW impedance (ON). When inhibit input is "L", it becomes HIGH impedance (OFF). Pin configuration is same as standard CMOS logic 4000 family.

### **■** Schematic Diagram







### ■ Absolute Maximum Ratings

|                | Parameter                      |                               | Symbol           | Rating                                    | Unit        |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
|----------------|--------------------------------|-------------------------------|------------------|-------------------------------------------|-------------|----------------|---------|------------------|---------|-------------|---------|------------|-----|------------------|---|---------------|--|----------------|--|----------------|--|-----------------|--|----------------|--|------------|------------------------------|---|
| Supply voltage | oply voltage                   |                               | tage             |                                           | ply voltage |                | voltage |                  | voltage |             | voltage |            | Vcc | $-0.5 \sim +7.0$ | V |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
| Input/output   | Input/output voltage           |                               |                  | output voltage                            |             | output voltage |         | t/output voltage |         | put voltage |         | ut voltage |     | itput voltage    |   | utput voltage |  | output voltage |  | output voltage |  | /output voltage |  | output voltage |  | $V_I, V_O$ | $-0.5 \sim \text{Vcc} + 0.5$ | V |
| Input protec   | Input protection diode current |                               |                  | ±20                                       | mA          |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
| Output paras   | Output parasitic diode current |                               |                  | ±20                                       | mA          |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
| Output curre   | Output current                 |                               |                  | ± 35                                      | mA          |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
| Supply curre   | rent                           |                               | $I_{CC,}I_{GND}$ | ±70                                       | mA          |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
| Storage tem    | perature range                 |                               | Tstg             | <b>-65∼+150</b>                           | °C          |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
|                | MANGALICAGE                    | $Ta = -40 \sim +60^{\circ}C$  | Pp               | 400                                       | mW          |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
| Power          | MN74HC4066                     | $Ta = +60 \sim +85^{\circ}C$  | r p              | Decrease to 200mW at the rate of 8mW/°C   | III VV      |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
| dissipation    | MN74 HC4066S                   | $Ta = -40 \sim +60^{\circ}C$  | $P_{D}$          | 275                                       | mW          |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |
|                | WIN 4 FIC4000S                 | $T_a = +60 \sim +85^{\circ}C$ | rp               | Decrease to 200mW at the rate of 3.8mW/°C | 111 VV      |                |         |                  |         |             |         |            |     |                  |   |               |  |                |  |                |  |                 |  |                |  |            |                              |   |

# ■ Operating Conditions

| Parameter                   | Symbol                          | Vcc(V) | Rating          | Unit |
|-----------------------------|---------------------------------|--------|-----------------|------|
| Operating supply voltage    | $V_{\rm cc}$                    |        | 2.0~6.0         | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |        | $0 \sim V_{CC}$ | v    |
| Operating temperature range | TA                              |        | -40~+85         | r    |
|                             |                                 | 2.0    | 0~1000          | ns   |
| Input rise and fall time    | t <sub>r</sub> , t <sub>f</sub> | 4.5    | 0~500           | ns   |
|                             |                                 | 6.0    | 0~400           | ns   |

|                               |          |      |                                                                           |       | Te     | mperat | ure      |         |      |
|-------------------------------|----------|------|---------------------------------------------------------------------------|-------|--------|--------|----------|---------|------|
| Parameter                     | Symbol   | Vcc  | Test Conditions                                                           | •     | Γa=25° | 2      | Ta = -40 | )~+85°C | Unit |
|                               |          | (V)  |                                                                           | min.  | typ.   | max.   | min.     | max.    |      |
|                               |          | 2. 0 |                                                                           | 1.5   |        |        | 1.5      |         | V    |
| Input HIGH voltage            | Vih      | 4.5  |                                                                           | 3. 15 |        |        | 3. 15    |         | V    |
|                               |          | 6.0  |                                                                           | 4. 2  |        |        | 4. 2     |         | V    |
|                               |          | 2. 0 |                                                                           |       |        | 0.3    |          | 0.3     | V    |
| Input LOW voltage             | VIL      | 4.5  |                                                                           |       |        | 0. 9   |          | 0.9     | V    |
|                               |          | 6.0  |                                                                           |       |        | 1.2    |          | 1.2     | V    |
| Input current                 | Iı       | 6.0  | V <sub>I</sub> = Vcc or GND                                               |       |        | ±0.1   |          | ±1.0    | μA   |
| Quiescent supply current      | Icc      | 6.0  | $V_{I} = V_{CC} \text{ or } GND$                                          |       |        | 2.0    |          | 20.0    | ^    |
| Quiescent supply current      | Tec      | 0.0  | $I_0 = 0$                                                                 |       |        | 2.0    |          | 20.0    | μΑ   |
| Input/output off reak current | I s(off) | 6.0  | $V_{I} = V_{IH} \text{ or } V_{IL}$<br>$ V_{S}  = V_{CC} \text{ or } GND$ |       |        | ±1.0   |          | ±0.1    | μΑ   |
|                               |          | 2. 0 |                                                                           |       | 1000   | 2000   |          | 3000    | Ω    |
| On resistance                 | Ron      | 3.0  | Vis: Vcc~GND                                                              |       | 200    | 400    |          | 600     | Ω    |
| On resistance                 | KON      | 4.5  | VIS · V CC ~ GND                                                          |       | 80     | 160    |          | 240     | Ω    |
|                               |          | 6.0  |                                                                           |       | 60     | 120    |          | 180     | Ω    |
|                               |          | 2.0  |                                                                           |       | 150    |        |          |         | Ω    |
| Variation of On resist-       | ΔRon     | 3. 0 |                                                                           |       | 25     |        |          |         | Ω    |
| ance                          | 1 A NON  | 4.5  |                                                                           |       | 10     |        |          |         | Ω    |
|                               |          | 6.0  |                                                                           |       | 7      |        |          |         | Ω    |

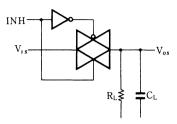


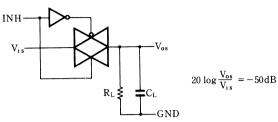
# ■ AC Characteristics (GND=0V, Input transition time $\leq$ 6ns, $C_L$ =50pF)

|                                              |        | $V_{CC}$          |                                                                                                                                                    |      | T      | emperati        | ıre    |                 |      |
|----------------------------------------------|--------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------|--------|-----------------|--------|-----------------|------|
| Parameter                                    | Symbol | (V)               | Test Conditions                                                                                                                                    | -    | Γa=25℃ |                 | Ta=-40 | )~+85°C         | Unit |
|                                              |        | (,,               |                                                                                                                                                    | min. | typ.   | max.            | min.   | max.            |      |
| Propagation time $(H \rightarrow L)$         | tPHL   | 2.0<br>4.5<br>6.0 | $R = 1 k\Omega$ $C_L = 50 pF$                                                                                                                      |      |        | 50<br>10<br>9   |        | 65<br>13<br>11  | ns   |
| Propagation time ( L → H)                    | tpLH   | 2.0<br>4.5<br>6.0 | INH=V <sub>CC</sub> Input transition time=15ns                                                                                                     |      |        | 50<br>10<br>9   |        | 65<br>13<br>11  | ns   |
| 3-state propagation time $(H \rightarrow Z)$ | tpHZ   | 2.0<br>4.5<br>6.0 | $R = 1 k\Omega$ $C_L = 50 pF$                                                                                                                      |      |        | 150<br>30<br>26 |        | 190<br>38<br>33 | ns   |
| 3-state propagation time $(Z \rightarrow H)$ | tpzh   | 2.0<br>4.5<br>6.0 | $Y = V_{CC}$ $R_{L} \rightarrow GND$                                                                                                               |      |        | 150<br>30<br>26 |        | 190<br>38<br>33 | ns   |
| 3-state propagation time $(L \rightarrow Z)$ | tPLZ   | 2.0<br>4.5<br>6.0 | $R_L=10 k\Omega$ $C_L=50 pF$                                                                                                                       |      |        | 150<br>30<br>26 |        | 190<br>38<br>33 | ns   |
| 3-state propagation time $(Z \rightarrow L)$ | tpzL   | 2.0<br>4.5<br>6.0 | $Y = \text{GND}$ $R_{L} \rightarrow V_{CC}$                                                                                                        |      |        | 150<br>30<br>26 |        | 190<br>38<br>33 | ns   |
| Sine Wave Distortion                         |        | 2.0<br>4.5<br>6.0 | $ \begin{array}{l} R_L \!\!=\! 10k\Omega \\ C_L \!\!=\! 50pF \\ f \!\! := \!\! 1kH_Z \\ Y \!\! = \!\! \frac{1}{2}V_{CC}(P \!\!-\! P) \end{array} $ |      | 0.1    |                 |        |                 | %    |
| Crosstalk<br>2 channel                       |        | 2.0<br>4.5<br>6.0 | $P_{L}=1k\Omega$ $Y=\frac{1}{2}V_{CC}(P-P)$                                                                                                        |      | t.b.f  |                 |        |                 | MHz  |
| Grosstalk INH $\rightarrow$ V <sub>SS</sub>  |        | 2.0<br>4.5<br>6.0 | $R_L=10k\Omega$ $C_L=50pF$ $INH=V_{CC}$                                                                                                            |      | t.b.f  |                 |        |                 | mV   |
| Feedthrough                                  |        | 2.0<br>4.5<br>6.0 | $\begin{array}{l} R_L \!\!=\! 1  k\Omega \\ C_L \!\!=\! 50 pF \\ I  NH \!\!=\! GND \\ Y \!\!=\! \frac{1}{2}  V_{CC}(P \!\!-\! P) \end{array}$      |      | t.b.f  |                 |        |                 | MHz  |
| Frequency Response                           |        | 2.0<br>4.5<br>6.0 | $R_L = 1k\Omega$ $INH = V_{CC}$                                                                                                                    |      | t.b.f  |                 |        |                 | MHz  |

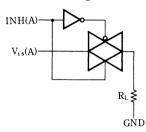
- · Switching Time Measuring Circuit and Waveforms
  - 1. Measuring Circuit (t<sub>PLH</sub>, t<sub>PHL</sub>)
    - (Fig. 1) Propagation Delay Time, Crosstalk Measuring circuit

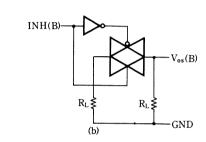
(Fig. 2) Sine Wave Distortion, Feedthrough Measuring Circuit



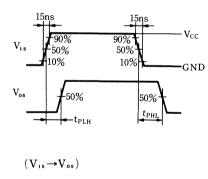


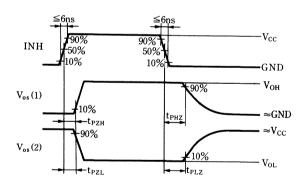
(Fig. 3) Crosstalk Measuring Circuit





### 2. Switching Time Waveforms





# MN74HC4075/MN74HC4075S

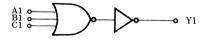
Triple 3-Input OR Gates

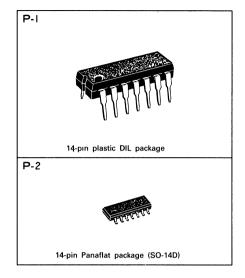
### **■** Description

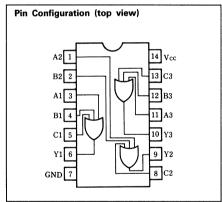
MN74HC4075/MN74HC4075S contain three 3-input positive isolation OR gate circuits.

Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard CMOS 4000 logic family.

### ■ Logic Diagram (1 gate)







### ■ Absolute Maximum Ratings

|                | Paramete                                             | r                            | Symbol          | Rating                                    | Unit   |                          |       |  |      |  |     |                  |   |
|----------------|------------------------------------------------------|------------------------------|-----------------|-------------------------------------------|--------|--------------------------|-------|--|------|--|-----|------------------|---|
| Supply voltage | ltage                                                |                              | ge              |                                           | ge     |                          | ltage |  | tage |  | Vcc | $-0.5 \sim +7.0$ | V |
| Input/output   | put voltage                                          |                              | voltage         |                                           | Vı, Vo | $-0.5 \sim V_{CC} + 0.5$ | V     |  |      |  |     |                  |   |
| Input protect  | tion diode current                                   |                              | I <sub>IK</sub> | ±20                                       | mA     |                          |       |  |      |  |     |                  |   |
| Output paras   | sitic diode current                                  |                              | Іок             | ±20                                       | mA     |                          |       |  |      |  |     |                  |   |
| Output curre   | ent                                                  | t                            |                 | ±25                                       | mA     |                          |       |  |      |  |     |                  |   |
| Supply curre   | ent                                                  | t                            |                 | ±50                                       | mA     |                          |       |  |      |  |     |                  |   |
| Storage tem    | perature range                                       |                              | Tstg            | <b>−65~+150</b>                           | °C     |                          |       |  |      |  |     |                  |   |
|                | ) (A) (G) (A) (G) (G) (G) (G) (G) (G) (G) (G) (G) (G | $Ta = -40 \sim +60^{\circ}C$ | D               | 400                                       | mW     |                          |       |  |      |  |     |                  |   |
| Power          | MN74 HC4075                                          | $Ta = +60 \sim +85^{\circ}C$ | $P_D$           | Decrease to 200mW at the rate of 8mW/°C   | mvv    |                          |       |  |      |  |     |                  |   |
| dissipation    | MANGA HOARE C                                        | $Ta = -40 \sim +60^{\circ}C$ | ъ               | 275                                       | 187    |                          |       |  |      |  |     |                  |   |
|                | MN74 HC4075 S                                        | $Ta = +60 \sim +85^{\circ}C$ | $P_D$           | Decrease to 200mW at the rate of 3.8mW/°C | mW     |                          |       |  |      |  |     |                  |   |

### **■** Operating Conditions

| Parameter                   | Symbol                          | $V_{CC}(V)$ | Rating              | Unit |
|-----------------------------|---------------------------------|-------------|---------------------|------|
| Operating supply voltage    | Vcc                             |             | 1.4~6.0             | V    |
| Input/output voltage        | Vı, Vo                          |             | $0 \sim V_{\rm CC}$ | v    |
| Operating temperature range | TA                              |             | $-40 \sim +85$      | °C   |
|                             |                                 | 2.0         | 0~1000              | ns   |
| Input rise and fall time    | t <sub>r</sub> , t <sub>f</sub> | 4.5         | 0~500               | ns   |
|                             |                                 | 6.0         | 0~400               | ns   |

# ■ DC Characteristics (GND=0V)

|                          |                 | 37                     | Tes         | st Conditio | ons       |      | ,       | Tempera | ture     |         |      |
|--------------------------|-----------------|------------------------|-------------|-------------|-----------|------|---------|---------|----------|---------|------|
| Parameter                | Symbol          | V <sub>cc</sub><br>(V) | Vı          | Io i        |           | 7    | Γa=25°0 | Ξ,      | Ta = -40 | )~+85°C | Unit |
|                          |                 | ( • )                  | VI          | 10          | Unit      | min. | typ.    | max.    | min.     | max.    |      |
|                          |                 | 2.0                    |             |             |           | 1.5  |         |         | 1.5      |         |      |
| Input HIGH voltage       | $V_{IH}$        | 4.5                    |             |             |           | 3.15 |         |         | 3.15     |         | V    |
|                          |                 | 6.0                    |             |             |           | 4.2  |         |         | 4.2      |         |      |
|                          |                 | 2.0                    |             |             |           |      |         | 0.3     |          | 0.3     |      |
| Input LOW voltage        | $V_{IL}$        | 4.5                    |             |             |           |      |         | 0.9     |          | 0.9     | V    |
|                          |                 | 6.0                    |             |             |           |      |         | 1.2     |          | 1.2     |      |
|                          |                 | 2.0                    |             | -20.0       | μA        | 1.9  | 2.0     |         | 1.9      |         |      |
|                          |                 | 4.5                    | VIH         | -20.0       | $\mu$ A   | 4.4  | 4.5     | ĺ       | 4.4      |         |      |
| Output HIGH voltage      | V <sub>OH</sub> | 6.0                    | or          | -20.0       | $\mu$ A   | 5.9  | 6.0     |         | 5.9      |         | V    |
|                          |                 | 4.5                    | VIL         | -4.0        | mΑ        | 3.86 |         |         | 3.76     |         |      |
|                          |                 | 6.0                    |             | -5.2        | mA        | 5.36 |         |         | 5.26     |         |      |
|                          |                 | 2.0                    |             | 20.0        | μA        |      | 0.0     | 0.1     |          | 0.1     |      |
|                          |                 | 4.5                    |             | 20.0        | μΑ        |      | 0.0     | 0.1     |          | 0.1     |      |
| Output LOW voltage       | Vol             | 6.0                    | VIL         | 20.0        | μΑ        |      | 0.0     | 0.1     |          | 0.1     | V    |
|                          |                 | 4.5                    | 1           | 4.0         | mA        |      |         | 0.32    |          | 0.37    |      |
|                          |                 | 6.0                    |             | 5.2         | mA        |      |         | 0.32    |          | 0.37    |      |
| Input current            | $I_{I}$         | 6.0                    | $V_I = V_C$ | c or GN     | D         |      |         | ±0.1    |          | ±1.0    | μA   |
| Quiescent supply current | $I_{CC}$        | 6.0                    | $V_I = V_C$ | or GNI      | $0,I_0=0$ |      |         | 2.0     |          | 20.0    | μA   |

# ■ AC Characteristics (GND=0V, Input transition time $\leq$ 6ns, $C_L$ =50pF)

|                           |                  |            |                 |      | Т       | emperati | ure      |         |      |
|---------------------------|------------------|------------|-----------------|------|---------|----------|----------|---------|------|
| Parameter                 | Symbol           | Vcc<br>(V) | Test Conditions | 7    | Γa=25°0 |          | Ta = -40 | )~+85°C | Unit |
|                           |                  | (*/        |                 | min. | typ.    | max.     | min.     | max.    |      |
|                           |                  | 2.0        |                 |      | 25      | 75       |          | 95      |      |
| Output rise time          | tTLH             | 4.5        |                 |      | 8       | 15       |          | 19      | ns   |
|                           |                  | 6.0        |                 |      | 7       | 13       |          | 16      |      |
|                           |                  | 2.0        |                 |      | 20      | 75       |          | 95      |      |
| Output fall time          | t <sub>THL</sub> | 4.5        |                 |      | 7       | 15       |          | 19      | ns   |
|                           |                  | 6.0        |                 |      | 6       | 13       |          | 16      |      |
|                           |                  | 2.0        |                 |      | 25      | 75       |          | 95      |      |
| Propagation time<br>(L→H) | tPLH             | 4.5        |                 |      | 8       | 15       |          | 19      | ns   |
| ( <b>D</b> 11)            |                  | 6.0        |                 |      | 7       | 13       |          | 16      |      |
|                           |                  | 2.0        |                 |      | 25      | 75       |          | 95      |      |
| Propagation time<br>(H→L) | tPHL             | 4.5        |                 |      | 8       | 15       |          | 19      | ns   |
| (11 12)                   |                  | 6.0        |                 |      | 7       | 13       |          | 16      |      |



# MN74HC4078/MN74HC4078S

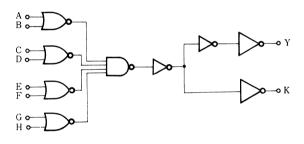
# 8-Input NOR Gate

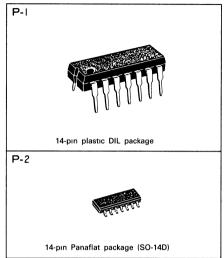
### **■** Description

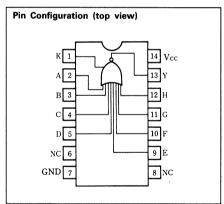
MN74HC4078/MN74HC4078S contain 8-input positive isolation NOR gate circuits.

Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in  $V_{\rm DD}$  and  $V_{\rm SS}$  for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard CMOS 4000 logic family.

### ■ Logic Diagram







### ■ Absolute Maximum Ratings

|                | Parameter           |                              |                | Rating                                    | Unit                            |                          |   |
|----------------|---------------------|------------------------------|----------------|-------------------------------------------|---------------------------------|--------------------------|---|
| Supply voltage | ge                  |                              | Vcc            | $-0.5 \sim +7.0$                          | V                               |                          |   |
| Input/output   | itput voltage       |                              | output voltage |                                           | V <sub>I</sub> , V <sub>O</sub> | $-0.5 \sim V_{CC} + 0.5$ | V |
| Input protec   | tion diode current  |                              | Iικ            | ±20                                       | mA                              |                          |   |
| Output paras   | sitic diode current |                              | Іок            | ±20                                       | mA                              |                          |   |
| Output curre   | ent                 |                              | Io             | ±25                                       | mA                              |                          |   |
| Supply curre   | ent                 |                              | ICC, IGND      | ±50                                       | mA                              |                          |   |
| Storage tem    | perature range      |                              | Tstg           | -65~+150                                  | °Ċ                              |                          |   |
| Ţ              |                     | $Ta = -40 \sim +60^{\circ}C$ | Ъ              | 400                                       | mW                              |                          |   |
| Power          | MN74HC4078          | Ta=+60~+85°C                 | $P_D$          | Decrease to 200mW at the rate of 8mW/°C   | m vv                            |                          |   |
| dissipation    | MNZALICAOZOS        | $Ta = -40 \sim +60^{\circ}C$ | D              | 275                                       | 337                             |                          |   |
|                | MN74 HC4078 S       | Ta=+60~+85°C                 | $P_D$          | Decrease to 200mW at the rate of 3.8mW/°C | mW                              |                          |   |

# ■ Operating Conditions

| Parameter                   | Symbol                          | V <sub>CC</sub> (V) | Rating              | Unit |
|-----------------------------|---------------------------------|---------------------|---------------------|------|
| Operating supply voltage    | $V_{\rm cc}$                    |                     | 1.4~6.0             | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |                     | $0 \sim V_{\rm CC}$ | v    |
| Operating temperature range | TA                              |                     | $-40 \sim +85$      | °C   |
|                             |                                 | 2.0                 | 0~1000              | ns   |
| Input rise and fall time    | t <sub>r</sub> , t <sub>f</sub> | 4.5                 | 0~500               | ns   |
|                             |                                 | 6.0                 | 0~400               | ns   |

### ■ DC Characteristics (GND=0V)

|                          |                 |     | Tes               | st Conditio | ons       |         |      | Tempera | iture          |      |      |
|--------------------------|-----------------|-----|-------------------|-------------|-----------|---------|------|---------|----------------|------|------|
| Parameter                | Symbol          | (V) | $(V)$ $V_{\rm I}$ |             |           | Ta=25°C |      |         | Ta=-40°C~+85°C |      | Unit |
|                          |                 | ,   | V I               | Io          | Unit      | min.    | typ. | max.    | min.           | max. |      |
|                          |                 | 2.0 |                   |             |           | 1.5     |      |         | 1.5            |      |      |
| Input HIGH voltage       | V <sub>IH</sub> | 4.5 |                   |             |           | 3.15    |      |         | 3.15           |      | V    |
|                          |                 | 6.0 |                   |             |           | 4.2     |      |         | 4.2            |      |      |
|                          |                 | 2.0 |                   |             |           |         |      | 0.3     |                | 0.3  |      |
| Input LOW voltage        | $V_{IL}$        | 4.5 |                   |             |           |         |      | 0.9     |                | 0.9  | V    |
|                          |                 | 6.0 |                   |             |           |         |      | 1.2     |                | 1.2  |      |
|                          |                 | 2.0 |                   | -20.0       | μA        | 1.9     | 2.0  | 0.1     | 1.9            | 0.1  |      |
|                          |                 | 4.5 | VIH               | -20.0       | μA        | 4.4     | 4.5  | 0.1     | 4.4            | 0.1  |      |
| Output HIGH voltage      | V <sub>OH</sub> | 6.0 | or                | -20.0       | μA        | 5.9     | 6.0  | 0.1     | 5.9            | 0.1  | V    |
|                          |                 | 4.5 | VIL               | -4.0        | mA        | 3.86    |      | 0.32    | 3.76           | 0.37 |      |
|                          |                 | 6.0 |                   | -5.2        | mA        | 5.36    |      | 0.32    | 5.26           | 0.37 |      |
|                          |                 | 2.0 |                   | 20.0        | μA        |         | 0.0  | 0.1     |                | 0.1  |      |
|                          |                 | 4.5 | $V_{IH}$          | 20.0        | μA        |         | 0.0  | 0.1     |                | 0.1  |      |
| Output LOW voltage       | Voi             | 6.0 | or                | 20.0        | μA        |         | 0.0  | 0.1     |                | 0.1  | V    |
|                          |                 | 4.5 | VIL               | 4.0         | mA        |         |      | 0.32    |                | 0.37 |      |
| •                        |                 | 6.0 |                   | 5.2         | mA        |         |      | 0.32    |                | 0.37 |      |
| Input current            | II              | 6.0 | $V_1 = V_0$       | c or GN     | D         |         |      | ±0.1    |                | ±1.0 | μA   |
| Quiescent supply current | $I_{CC}$        | 6.0 | $V_I = V_C$       | c or GNI    | $0,I_0=0$ | 1       |      | 2.0     |                | 20.0 | μA   |

### ■ AC Characteristics (GND=0V, Input transition time ≤6ns, C<sub>L</sub>=50pF)

|                           |                  |                     |                 |      | •      | Γempera | ture  |         |      |
|---------------------------|------------------|---------------------|-----------------|------|--------|---------|-------|---------|------|
| Parameter                 | Symbol           | V <sub>CC</sub> (V) | Test Conditions | ·    | Γa=25° | С       | Ta=-4 | )~+85°C | Unit |
|                           |                  | ( , ,               |                 | min. | typ.   | max.    | mın.  | max.    |      |
|                           |                  | 2.0                 |                 |      | 25     | 75      |       | 95      |      |
| Output rise time          | tTLH             | 4.5                 |                 |      | 8      | 15      |       | 19      | ns   |
|                           |                  | 6.0                 |                 |      | 7      | 13      |       | 16      |      |
|                           |                  | 2.0                 |                 |      | 20     | 75      |       | 95      |      |
| Output fall time          | t <sub>THL</sub> | 4.5                 |                 |      | 7      | 15      |       | 19      | ns   |
|                           |                  | 6.0                 |                 |      | 6      | 13      |       | 16      |      |
| 70                        |                  | 2.0                 |                 |      |        | 125     |       | 155     |      |
| Propagation time<br>(L→H) | tPLH             | 4.5                 |                 |      | 15     | 25      |       | 31      | ns   |
| (1)                       |                  | 6.0                 |                 |      |        | 21      |       | 26      |      |
| D                         |                  | 2.0                 |                 |      |        | 125     |       | 155     |      |
| Propagation time<br>(H→L) | t <sub>PHL</sub> | 4.5                 |                 |      | 13     | 25      |       | 31      | ns   |
|                           |                  | 6.0                 |                 |      |        | 21      |       | 26      |      |



# MN74HC4301/MN74HC4301S

TTL Input Octal TRI-STATE Latch with Inverting Outputs

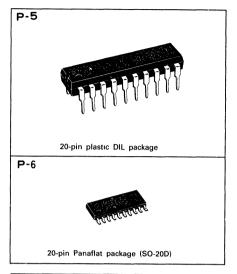
### ■ Description

MN74HC4301/MN74HC4301S contain TTL input octal tri-state latches with inverting outputs. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more logic "1". High output driving capacity and tri-state output driving capacity and tri-state output are suited for the use of common bus line in the bus utilized system. When output disable input is "L", and latch enable input is "H", data input is inverted and transferred to output.

When latch enable is "L", data input is maintained as is until when latch enable input becomes "H" again.

When output disable input is "H", all outputs become high impedance state regardless of other inputs or data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directry driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



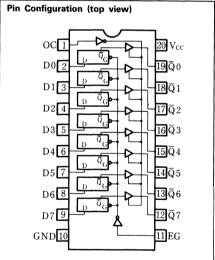
# ■ Truth Table

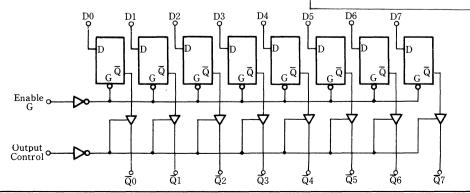
| Output Control | Enable | D | Output |
|----------------|--------|---|--------|
| L              | Н      | Н | L      |
| L              | Н      | L | Н      |
| L              | L      | × | $Q_0$  |
| Н              | ×      | × | Hi-Z   |

### Note:

- 1. ×: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance
- 3.  $Q_0$ : Q level prior to determination of input condition shown in table

# ■ Logic Diagram





# ■ Absolute Maximum Ratings

|               | Paramete                                       | er           | Symbol                             | Rating                                    | Unit                   |    |     |    |
|---------------|------------------------------------------------|--------------|------------------------------------|-------------------------------------------|------------------------|----|-----|----|
| Supply voltag | voltage .                                      |              | $V_{\rm CC}$                       | $-0.5 \sim +7.0$                          | V                      |    |     |    |
| Input/output  | voltage                                        |              | V <sub>I</sub> , V <sub>O</sub>    | $-0.5 \sim V_{\rm CC} + 0.5$              | V                      |    |     |    |
| Input protec  | tion diode current                             |              | Iıĸ                                | ±20                                       | mA                     |    |     |    |
| Output paras  | Output parasitic diode current                 |              |                                    | ±20                                       | mA                     |    |     |    |
| Output curre  | Output current                                 |              |                                    | current                                   |                        | Io | ±35 | mA |
| Supply curre  | ent                                            |              | I <sub>CC</sub> , I <sub>GND</sub> | ± 70                                      | mA                     |    |     |    |
| Storage tem   | perature range                                 |              | Tstg                               | -65~+150                                  | $^{\circ}\!\mathbb{C}$ |    |     |    |
|               | 10/54 HQ4001                                   | Ta=-40~+60°C | $P_{D}$                            | 400                                       | 117                    |    |     |    |
| Power         | Power MN74 HC4301 $T_a = +60 \sim +85^{\circ}$ |              | PD                                 | Decrease to 200mW at the rate of 8mW/°C   | mW                     |    |     |    |
| dissipation   |                                                |              | D                                  | 275                                       | mW                     |    |     |    |
|               | MN74 HC4301 S                                  | Ta=+60~+85℃  | $P_{D}$                            | Decrease to 200mW at the rate of 3.8mW/°C | m vv                   |    |     |    |

### **■** Operating Conditions

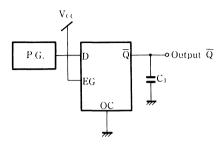
| Parameter                   | Symbol                          | V <sub>cc</sub> (V) | Rating              | Unit |
|-----------------------------|---------------------------------|---------------------|---------------------|------|
| Operating supply voltage    | Vcc                             |                     | 4.5~5.5             | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |                     | $0{\sim}V_{\rm CC}$ | V    |
| Operating temperature range | TA                              |                     | -40~+85             | °C   |
| Input rise and fall time    | tr, tf                          | 4.5                 | 0~500               | ns   |

|                                  | ***             |             | Test Conditions       |           |           | Т    | `empera | ture  |       |           |      |
|----------------------------------|-----------------|-------------|-----------------------|-----------|-----------|------|---------|-------|-------|-----------|------|
| Parameter                        | Symbol          | V cc<br>(V) | Vı                    | Io ,      |           |      | Γa=25°  | 2     | Ta=-4 | 0~+85℃    | Unit |
|                                  |                 | ( • )       |                       | 10        | Unit      | min. | typ.    | max.  | mın.  | max.      |      |
|                                  |                 | 4.5         |                       |           |           |      |         |       |       |           |      |
| Input HIGH voltage               | Vih             | \$          |                       |           |           | 2.0  |         |       | 2. 0  |           | V    |
|                                  |                 | 5. 5        |                       | !         |           |      |         |       |       |           |      |
|                                  |                 | 4.5         |                       |           |           |      |         |       |       |           |      |
| Input LOW voltage                | VIL             | 5           |                       |           |           |      |         | 0.8   |       | 0.8       | V    |
|                                  |                 | 5. 5        |                       |           |           |      |         |       |       |           |      |
| Output IIICII velte co           | V <sub>OH</sub> | 4.5         | VIH                   | -20.0     | μΑ        | 4.4  | 4.5     |       | 4.4   |           | V    |
| Output HIGH voltage              |                 | 4.5         | or<br>V <sub>IL</sub> | - 6.0     | mA        | 3.86 |         |       | 3. 76 |           | V    |
| 0                                | 17              | 4.5         | VIH                   | 20. 0     | μA        |      | 0. 0    | 0. 1  |       | 0.1       | V    |
| Output LOW voltage               | Vol             | 4.5         | VIL                   | 6.0       | mA        |      |         | 0. 32 |       | 0.37      | V    |
| Input current                    | I <sub>1</sub>  | 5.5         | V 1=Vc                | or GND    |           |      |         | ±0.1  |       | $\pm 1.0$ | μA   |
| 3-state output off state current | I <sub>OZ</sub> | 5.5         | 1                     | IH or VIL |           |      |         | ±0.5  |       | ± 5.0     | μΑ   |
| Quiescent supply current         | I cc            | 5. 5        | $V_I = V_C$           | c or GND  | $I_0 = 0$ |      |         | 8. 0  |       | 80.0      | μA   |

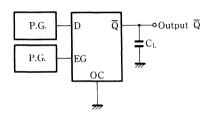
# $\blacksquare$ AC Characteristics (GND=0V, Input transition time $\leqq\!6ns,~C_L\!=\!50pF\!)$

|                                                                       |                    |     |                    |      | Tempera | ature C | Condition | n      |      |
|-----------------------------------------------------------------------|--------------------|-----|--------------------|------|---------|---------|-----------|--------|------|
| Parameter                                                             | Symbol             | Vcc | Test Conditions    | ,    | Γa=25℃  |         | Ta=-4     | 0~+85℃ | Unit |
|                                                                       |                    | (V) |                    | min. | typ.    | max.    | min.      | max.   |      |
| Output rise time                                                      | t <sub>TLH</sub>   | 4.5 |                    |      | 8       | 15      |           | 19     | ns   |
| Output fall time                                                      | tгні.              | 4.5 |                    |      | 7       | 15      |           | 19     | ns   |
| Propagation time $D \rightarrow \overline{Q} (L \rightarrow H)$       | tРLН               | 4.5 |                    |      | 10      | 20      |           | 25     | ns   |
| Propagation time $D \rightarrow \overline{Q} (H \rightarrow L)$       | t <sub>PHI</sub> . | 4.5 |                    |      | 14      | 25      |           | 31     | ns   |
| Propagation time enable $G \rightarrow \overline{Q}(L \rightarrow H)$ | tPLH               | 4.5 |                    |      | 12      | 25      |           | 31     | ns   |
| Propagation time enable $G \rightarrow \overline{Q}(H \rightarrow L)$ | tphi.              | 4.5 |                    |      | 17      | 30      |           | 38     | ns   |
| 3-state propagation time $(H \rightarrow Z)$                          | tpHZ.              | 4.5 | $R_L = 1k\Omega$   |      | 15      | 25      |           | 31     | ns   |
| 3-state propagation time $(L \rightarrow Z)$                          | <b>t</b> PLZ       | 4.5 | $R_I = 1 k \Omega$ |      | 15      | 25      |           | 31     | ns   |
| 3-state propagation time $(Z \rightarrow H)$                          | tрzн               | 4.5 | $R_1 = 1k\Omega$   |      | 10      | 20      |           | 25     | ns   |
| 3-state propagation time $(Z \rightarrow L)$                          | tp/1               | 4.5 | $R_1 = 1k\Omega$   |      | 18      | 30      |           | 38     | ns   |

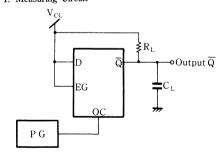
- Switching Time Measuring Circuit and Waveforms
- [1]  $t_{TLH}$ ,  $t_{THL}$ ,  $t_{PLH}/t_{PHL}(D \rightarrow \overline{Q})$ 
  - 1. Measuring Circuit



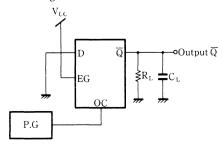
- (2)  $t_{PLH}/t_{PHL} (EG \rightarrow \overline{Q})$ 
  - 1. Measuring Circuit



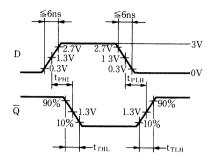
- (3) tphz, tpzH
  - 1. Measuring Circuit



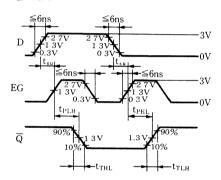
- (4) tPLZ, tPZL
  - 1. Measuring Circuit



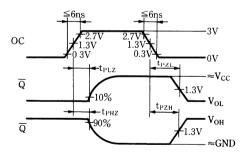
### 2. Waveforms



### 2. Waveforms



### 2. Waveforms



### 2. Waveforms

See above [3] 2. for waveforms.



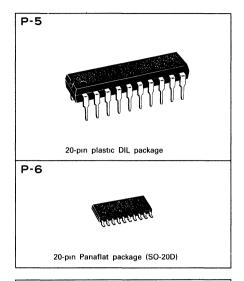
# MN74HC4302/MN74HC4302S

# TTL Input Octal TRI-STATE Latches

### ■ Description

MN74HC4302/MN74HC4302S contain TTL input octal tri-state latches with outputs. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more logic "1". High output driving capacity and tri-state output driving capacity and tri-state output driving capacity and tri-state output are suited for the use of common bus line in the bus utilized system. When output disable input is "L", and latch enable input is "H", data input is inverted and transferred to output. When latch enable is "L", data input is maintained as is until when latch enable input becomes "H" again.

When output disable input is "H", all outputs become high impedance state regardless of other inputs or data hold circuits. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directry driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



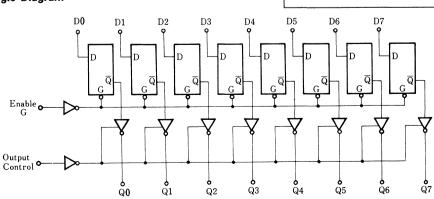
### **■** Truth Table

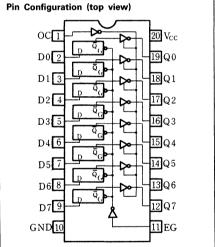
| Output Control | Enable G | D | Output |
|----------------|----------|---|--------|
| L              | Н        | Н | Н      |
| L              | Н        | L | L      |
| L              | L        | × | $Q_0$  |
| Н              | ×        | × | Hi-Z   |

#### Note:

- 1. x: Either HIGH or LOW; it doesn't matter
- 2. Hi-Z: High impedance
- 3. Q<sub>O</sub>: Q level prior to determination of input condition shown in table

### **■** Logic Diagram





# ■ Absolute Maximum Ratings

|                           | Paramete                     | r           | Symbol                             | Rating                                    | Unit          |    |     |    |
|---------------------------|------------------------------|-------------|------------------------------------|-------------------------------------------|---------------|----|-----|----|
| Supply voltage            | upply voltage                |             | $V_{\rm cc}$                       | $-0.5 \sim +7.0$                          | V             |    |     |    |
| Input/output              | voltage                      |             | V <sub>I</sub> , V <sub>O</sub>    | -0.5~V <sub>cc</sub> +0.5                 | v             |    |     |    |
| Input protec              | tion diode current           |             | I <sub>IK</sub>                    | ±20                                       | mA            |    |     |    |
| Output paras              | tput parasitic diode current |             |                                    | ±20                                       | mA            |    |     |    |
| Output curre              | Output current               |             |                                    | put current                               |               | Io | ±35 | mA |
| Supply curre              | ırrent                       |             | I <sub>CC</sub> , I <sub>GND</sub> | ± 70                                      | mA            |    |     |    |
| Storage tem               | perature range               |             | Tstg                               | <b>−65∼+150</b>                           | ${\mathbb C}$ |    |     |    |
|                           | MN74 HC4302                  | Ta=-40~+60℃ | Pp                                 | 400                                       | mW            |    |     |    |
| Power Power               |                              | Ta=+60~+85℃ | ] r-D                              | Decrease to 200mW at the rate of 8mW/°C   | ın vv         |    |     |    |
| dissipation MN74 HC4302 S |                              |             |                                    | 275                                       | mW            |    |     |    |
|                           | MIN/4HC43025                 | Ta=+60~+85℃ | P <sub>D</sub>                     | Decrease to 200mW at the rate of 3.8mW/°C | mW            |    |     |    |

# **■** Operating Conditions

| Parameter                   | Symbol                          | V <sub>CC</sub> | Rating            | Unit |
|-----------------------------|---------------------------------|-----------------|-------------------|------|
| Operating supply voltage    | $V_{\rm CC}$                    |                 | 4.5~5.5           | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |                 | 0~V <sub>cc</sub> | V    |
| Operating temperature range | T <sub>A</sub>                  |                 | <b>−40~+85</b>    | °C   |
| Input rise and fall time    | t <sub>r</sub> , t <sub>f</sub> | 4.5V            | 0~500             | ns   |

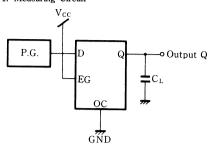
|                          |          |                     | Tes                           | st Conditio | ns        |      | Te     | mperati | ıre     |        |             |
|--------------------------|----------|---------------------|-------------------------------|-------------|-----------|------|--------|---------|---------|--------|-------------|
| Parameter                | Symbol   | V <sub>CC</sub> (V) | V <sub>1</sub> I <sub>0</sub> | Ι.          |           |      | Γa=25° | 2       | Ta = -4 | 0~+85℃ | Unit        |
|                          |          |                     |                               | 10          | Unit      | min. | typ.   | max.    | min.    | max.   |             |
| Input HIGH voltage       |          | 4.5                 |                               |             |           |      |        |         |         |        |             |
|                          | $V_{1H}$ | 5                   |                               |             |           | 2.0  |        |         | 2. 0    |        | V           |
|                          |          | 5. 5                |                               |             |           |      |        |         |         |        |             |
|                          |          | 4.5                 |                               |             |           |      |        |         |         |        |             |
| Input LOW voltage        | $V_{11}$ | 5                   |                               |             |           |      |        | 0.8     |         | 0.8    | V           |
|                          |          | 5. 5                |                               |             |           |      |        |         |         |        |             |
|                          | Vон      | 4.5                 | VIH                           | -20.0       | μA        | 4.4  | 4.5    |         | 4.4     |        | V           |
| Output HIGH voltage      |          | 4.5                 | or<br>V <sub>11</sub>         | - 6.0       | mA        | 3.86 |        |         | 3. 76   |        | V           |
|                          |          | 4.5                 | Vih                           | 20. 0       | μΑ        |      | 0.0    | 0. 1    |         | 0.1    | V           |
| Output LOW voltage       | Voi      | 4.5                 | or<br>V <sub>IL</sub>         | 6. 0        |           |      |        | 0. 32   |         | 0. 37  | V           |
| Input current            | Ιı       | 5. 5                | V 1=Vc                        | or GND      |           |      |        | ±0.1    |         | ±1.0   | μA          |
| 3-state output off state | Ioz      | 5.5                 | V I = V                       | IH or VIL   |           |      |        | ±0.5    |         | ± 5. 0 | μΑ          |
| current                  | 10%      | 5. 5                | $V_0 = V$                     | Vcc or GND  |           |      |        | _ 0. 3  |         | _ 5.0  | <i>~</i> 11 |
| Quiescent supply current | Icc      | 5.5                 | $V_1 = V_0$                   | c or GND    | $I_0 = 0$ |      |        | 8. 0    |         | 80. 0  | μA          |



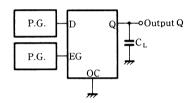
### ■ AC Characteristics (GND=0V, Input transition time ≦6ns, C<sub>L</sub>=50pF)

|                                                            |              | 37                  |                  |      | 7      | Tempera | ture     |        |      |
|------------------------------------------------------------|--------------|---------------------|------------------|------|--------|---------|----------|--------|------|
| Parameter                                                  | Symbol       | V <sub>CC</sub> (V) | Test Conditions  |      | Γa=25℃ |         | Ta = - 4 | 0~+85℃ | Unit |
|                                                            |              | (*)                 |                  | min. | typ.   | max.    | min.     | max.   |      |
| Output rise time                                           | tтLн         | 4.5                 |                  |      | 7      | 15      |          | 19     | ns   |
| Output fall time                                           | tтнL         | 4.5                 |                  |      | 6      | 15      |          | 19     | ns   |
| Propagation time<br>D→Q (L→H)                              | tрLн         | 4.5                 |                  |      | 11     | 20      |          | 25     | ns   |
| Propagation time $D \rightarrow Q (H \rightarrow L)$       | tPHL         | 4.5                 |                  |      | 16     | 30      |          | 38     | ns   |
| Propagation time enable $G \rightarrow Q(L \rightarrow H)$ | tрLн         | 4.5                 |                  |      | 15     | 25      |          | 31     | ns   |
| Propagation time enable $G \rightarrow Q(H \rightarrow L)$ | tpHL         | 4.5                 |                  |      | 15     | 25      |          | 31     | ns   |
| 3-state propagation time $(H \rightarrow Z)$               | tрнz         | 4.5                 | $R_L = 1k\Omega$ |      | 10     | 25      |          | 31     | ns   |
| 3-state propagation time $(L \rightarrow Z)$               | tplZ         | 4.5                 | $R_L = 1k\Omega$ |      | 16     | 30      |          | 38     | ns   |
| 3-state propagation time $(Z \rightarrow H)$               | tрzн         | 4.5                 | $R_L = 1k\Omega$ |      | 9      | 20      |          | 25     | ns   |
| 3-state propagation time $(Z \rightarrow L)$               | <b>t</b> PZL | 4.5                 | $R_L = 1k\Omega$ |      | 18     | 30      |          | 38     | ns   |

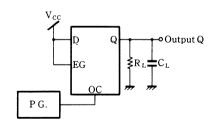
- Switching Time Measuring Circuit and Waveforms
  - (1)  $t_{TLH}$ ,  $t_{THL}$ ,  $t_{PLH}/t_{PHL}(D\rightarrow Q)$ 
    - 1. Measuring Circuit



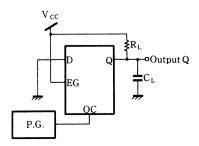
- [2]  $t_{PLH}/t_{PHL}(ENG\rightarrow Q)$ 
  - 1. Measuring Circuit



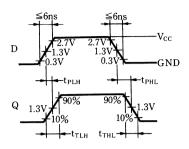
- . [3] tpHZ, tpZH
  - 1. Measuring Circuit



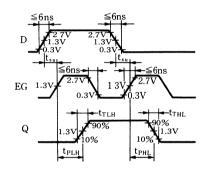
- (4) tplz, tpzl
  - 1. Measuring Circuit



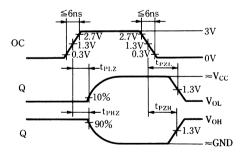
### 2. Waveforms



### 2. Waveforms



### 2. Waveforms



### 2. Waveforms

See above [3] 2. for waveforms.



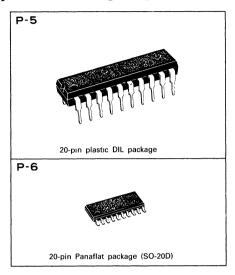
# MN74HC4303/MN74HC4303S

TTL Input Octal TRI-STATE D-Type Flip-Flops with Inverting Outputs

### **■** Description

MN74HC4303/MN74HC3403S are TTL input octal tri-state D-type flip-flop with inverting outputs. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more logic "1". High output driving capacity and tri-state output are suited for the use of common bus line in the bus utilized system D input data satisfying set-up time is inverted by the rising edge of clock input and trasferred to output. When output disable input is "H", all outputs become high impedance regardless of other inputs or data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



### **■** Truth Table

| In             | Input                |   |       |  |  |  |  |  |
|----------------|----------------------|---|-------|--|--|--|--|--|
| Output Control | Output Control CLK D |   |       |  |  |  |  |  |
| L              | 5                    | Н | L     |  |  |  |  |  |
| L              | £                    | L | Н     |  |  |  |  |  |
| L              | L                    | × | $Q_0$ |  |  |  |  |  |
| Н              | ×                    | × | Hi-Z  |  |  |  |  |  |

#### Note:

1. 1: Data input is transferred to output on the positive-going

edge from LOW to HIGH of the clock

2. ×: Either HIGH or LOW; it doesn't matter

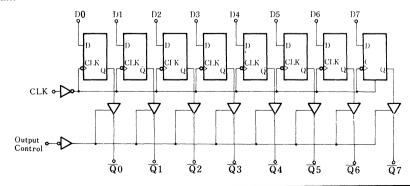
3.  $Q_0$ : Q level prior to determination of input condition shown in

table

4. Hi-Z: High impedance

# Pin Configuration (top view) $20 V_{CC}$ 19 **Q**0 D0 18 Q1 D117 Q2 D2 4 D3[5 $\overline{16}$ $\overline{Q}3$ $\overline{15}$ $\overline{Q}4$ 14 Q5 $\overline{13} \overline{Q} 6$ 12 **Q**7 D7 III CLK GND[10

#### ■ Logic Diagram



# ■ Absolute Maximum Ratings

|                                 | Parameter            | -                          | Symbol                             | Rating                                    | Unit       |    |      |    |
|---------------------------------|----------------------|----------------------------|------------------------------------|-------------------------------------------|------------|----|------|----|
| Supply voltage                  | y voltage            |                            | $V_{CC}$                           | <b>−0.5∼+7.0</b>                          | V          |    |      |    |
| Input/output                    | t voltage            |                            | V <sub>I</sub> , V <sub>O</sub>    | $-0.5 \sim V_{\rm CC} + 0.5$              | V          |    |      |    |
| Input protec                    | tion diode current   |                            | I <sub>IK</sub>                    | ±20                                       | mA         |    |      |    |
| Output paras                    | sitic diode current  |                            | Iok                                | ±20                                       | mA         |    |      |    |
| Output curre                    | Output current       |                            |                                    | t current                                 |            | Io | ± 35 | mA |
| Supply curre                    | rent                 |                            | I <sub>CC</sub> , I <sub>GND</sub> | ± 70                                      | mA         |    |      |    |
| Storage tem                     | ge temperature range |                            | Tstg                               | <del>-65</del> ∼+150                      | $^{\circ}$ |    |      |    |
|                                 | M N74 HC4303         | Ta=-40~+60℃                | $P_{D}$                            | 400                                       | mW         |    |      |    |
| Power Power                     |                      | Ta=+60~+85℃                | FD                                 | Decrease to 200mW at the rate of 8mW/°C   | m w        |    |      |    |
| dissipation MN74 HC4303S Ta=-40 |                      | $T_{a} = -40 \sim +60 $ °C |                                    | 275                                       | W          |    |      |    |
|                                 | 14111411043033       | Ta=+60~+85℃                | $P_{D}$                            | Decrease to 200mW at the rate of 3.8mW/°C | mW         |    |      |    |

### **■** Operating Conditions

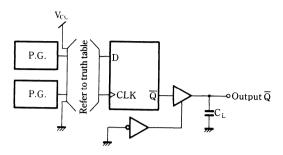
| Parameter                   | Symbol                          | Vcc(V) | Rating            | Unit |
|-----------------------------|---------------------------------|--------|-------------------|------|
| Operating supply voltage    | $V_{CC}$                        |        | 4.5~5.5           | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |        | 0~V <sub>cc</sub> | V    |
| Operating temperature range | TA                              |        | -40~+85           | °C   |
| Input rise and fall time    | t <sub>r</sub> , t <sub>f</sub> | 4.5    | 0~500             | ns   |

|                                  |          | V           | Tes                                                       | st Conditio | ns   |       | Т      | emperati | ıre      |        |      |
|----------------------------------|----------|-------------|-----------------------------------------------------------|-------------|------|-------|--------|----------|----------|--------|------|
| Parameter                        | Symbol   | V cc<br>(V) | Vı                                                        | Io          |      | 7     | Γa=25° |          | $T_a=-4$ | 0~+85℃ | Unit |
|                                  |          | (V)         |                                                           | 10          | Unit | min.  | typ.   | max.     | min.     | max.   |      |
|                                  |          | 4.5         |                                                           |             |      |       |        |          |          |        |      |
| Input HIGH voltage               | Vih      | \$          |                                                           |             |      | 2.0   |        |          | 2.0      |        | V    |
|                                  |          | 5. 5        |                                                           |             |      |       |        |          |          |        |      |
| Input LOW voltage                |          | 4.5         |                                                           |             |      |       |        |          |          | 1      |      |
|                                  | VIL      | S           |                                                           |             |      |       |        | 0.8      |          | 0.8    | V    |
|                                  |          | 5.5         |                                                           |             |      |       |        |          |          |        |      |
|                                  | Vон      | 4.5         | VIH                                                       | -20.0       | μA   | 4. 4  | 4. 5   |          | 4. 4     |        | v    |
| Output HIGH voltage              |          | 4.5         | or<br>V <sub>IL</sub>                                     | - 6.0       | mA   | 3. 86 |        |          | 3. 76    |        | v    |
|                                  |          | 4.5         | VIH                                                       | 20. 0       | μA   |       | 0.0    | 0. 1     |          | 0. 01  | v    |
| Output LOW voltage               | Vol      | 4.5         | or<br>V <sub>IL</sub>                                     | 6. 0        | mA   |       |        | 0. 32    |          | 0. 37  | v    |
| Input current                    | Iı       | 5.5         | V 1=Vc                                                    | or GND      |      |       |        | ±0.1     |          | 1.0    | μA   |
| 3-state output off state current | Ioz      | 5. 5        | $V_1 = V_{1H}$ or $V_{1I}$                                |             |      |       | ±0.5   |          | ± 5. 0   | μΑ     |      |
| Quiescent supply current         | $I_{CC}$ | 5. 5        | $V_0 = V_{CC}$ or GND<br>$V_1 = V_{CC}$ or GND, $I_0 = 0$ |             |      |       |        | 8.0      |          | 80.0   | μΑ   |

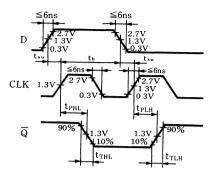
# ■ AC Characteristics (GND=0V, Input transition time $\leq$ 6ns, $C_L$ =50pF)

|                                                                    |                  | Vcc  |                    | _    | Т      | emperat | ure         |        |      |
|--------------------------------------------------------------------|------------------|------|--------------------|------|--------|---------|-------------|--------|------|
| Parameter                                                          | Symbol           | (V)  | Test Conditions    | -    | Γa=25℃ |         | $T_a = -40$ | )~+85℃ | Unit |
|                                                                    |                  |      |                    | min. | typ.   | max.    | min.        | max.   |      |
| Output rise time                                                   | t <sub>TLH</sub> | 4. 5 |                    |      | 8      | 15      |             | 19     | ns   |
| Output fall time                                                   | t <sub>THL</sub> | 4. 5 |                    |      | 6      | 15      |             | 19     | ns   |
| Propagation time $CLK \rightarrow \overline{Q}  (L \rightarrow H)$ | t <sub>РLН</sub> | 4. 5 |                    |      | 13     | 30      |             | 38     | ns   |
| Propagation time $CLK \rightarrow \overline{Q}  (H \rightarrow L)$ | t <sub>PHL</sub> | 4. 5 |                    |      | 18     | 30      |             | 38     | ns   |
| 3-state propagation time (H→Z)                                     | tPHZ             | 4. 5 | $R_L = 1 k\Omega$  |      | 18     | 30      |             | 38     |      |
| 3-state propagation time (L→Z)                                     | tPLZ             | 4. 5 | $R_L=1 k\Omega$    |      | 15     | 25      |             | 31     | ns   |
| 3-state propagation time (Z→H)                                     | tрzн             | 4. 5 | $R_L = 1  k\Omega$ |      | 14     | 25      |             | 31     | ns   |
| 3-state propagation time $(Z\rightarrow L)$                        | tpzL             | 4. 5 | $R_L = 1 k\Omega$  |      | 14     | 25      |             | 31     | ns   |
| Minimum Set-up time                                                | tsu              | 4.5  |                    |      | 2      | 20      |             | 25     | ns   |
| Minimum Hold time                                                  | t <sub>h</sub>   | 4.5  |                    |      |        | 0       |             |        | ns   |
| Maximum clock frequency                                            | fmax             | 4.5  |                    | 30   | 79     |         | 24          |        | MHz  |

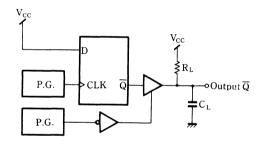
- Switching Time Measuring Circuit and Waveforms
- [1]  $t_{TLH}$ ,  $t_{THL}$ ,  $t_{su}$ ,  $f_{max}$ ,  $t_{PLH}$  /  $t_{PHL}$  (CLK $\rightarrow \overline{Q}$ )
  - 1. Measuring Circuit



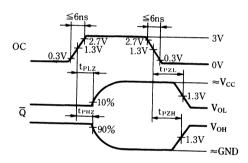
### 2. Waveforms



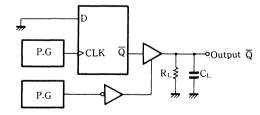
- (2) tpHZ, tpZH
  - 1. Measuring Circuit



### 2. Waveforms



- [3] tPLZ, tPZL
  - 1. Measuring Circuit



### 2. Waveforms

See above [3] 2. for waveforms.



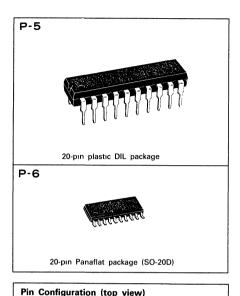
# MN74HC4304/MN74HC4304S

# TTL Input Octal TRI-STATE Flip-Flops

### ■ Description

MN74HC4304/MN74HC4304S are TTL input octal tri-state D type flip-flop. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more logic "1".

High output driving capacity and tri-state output are suited for the use of common bus line in the bus utilized system. D input data satisfying set-up time is transferred to output by the rising edge of clock input. When output disable input is "H", all outputs become high impedance regardless of other inputs or data hold circuits. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.



### ■ Truth Table

| In             | put |   | Output |
|----------------|-----|---|--------|
| Output Control | CLK | D | Q      |
| L              | 5   | Н | Н      |
| L              | f   | L | L      |
| L              | L   | × | $Q_0$  |
| Н              | ×   | × | Hi-Z   |

#### Note:

1. : Data input is transferred to output on the positive-going edge from LOW to HIGH of the clock

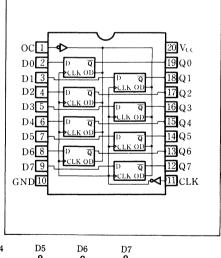
2. ×: Either HIGH or LOW; it doesn't matter

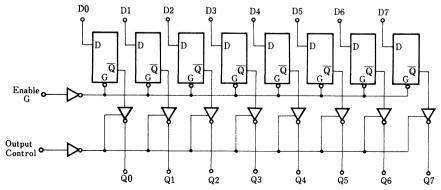
3. Q<sub>O</sub>: Q level prior to determination of input condition shown in

table

4. Hi-Z: High impedance

# ■ Logic Diagram





### ■ Absolute Maximum Ratings

|                | Parameter           | r            | Symbol                          | Rating                                    | Unit                 |
|----------------|---------------------|--------------|---------------------------------|-------------------------------------------|----------------------|
| Supply voltag  | ge                  |              | $V_{\rm CC}$                    | -0.5~+7.0                                 | V                    |
| Input/output   | voltage             |              | V <sub>I</sub> , V <sub>O</sub> | $-0.5 \sim V_{CC} + 0.5$                  | V                    |
| Input protec   | tion diode current  |              | I <sub>IK</sub>                 | $\pm 20$                                  | mA                   |
| Output paras   | sitic diode current |              | I <sub>OK</sub>                 | ±20                                       | mA                   |
| Output current |                     |              | Io                              | ±35                                       | mA                   |
| Supply curre   | Supply current      |              |                                 | ±70                                       | mA                   |
| Storage tem    | perature range      |              | Tstg                            | <del>-65~+150</del>                       | $^{\circ}\mathbb{C}$ |
|                | MANGALINIAGOA       | Ta=-40~+60℃  | $P_{D}$                         | 400                                       | mW                   |
| Power          | MN74 HN4304         | Ta=+60~+85℃  | l rp                            | Decrease to 200mW at the rate of 8mW/°C   | m w                  |
| dissipation    | MN74 HC4304 S       | Ta=-40~+60°C | $P_{D}$                         | 275                                       | mW                   |
|                | MINT4 II C4304 5    | Ta=+60~+85°C | I FD                            | Decrease to 200mW at the rate of 3.8mW/°C | III VV               |

## **■** Operating Conditions

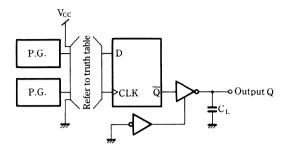
| Parameter                   | Symbol                          | Vcc(V) | Rating          | Unit |
|-----------------------------|---------------------------------|--------|-----------------|------|
| Operating supply voltage    | $V_{\rm CC}$                    |        | 4.5~5.5         | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |        | $0 \sim V_{CC}$ | V    |
| Operating temperature range | $T_{A}$                         |        | -40~+85         | °C   |
| Input rise and fall time    | t <sub>r</sub> , t <sub>f</sub> | 4.5 V  | 0~500           | ns   |

|                                  | Symbol          | 3.7  | Tes                                                 | st Conditio | ns   |      | •      | Гетрега | ture       |        |      |
|----------------------------------|-----------------|------|-----------------------------------------------------|-------------|------|------|--------|---------|------------|--------|------|
| Parameter                        |                 | (V)  |                                                     | Io ,        |      |      | Ta=25° | C       | $T_a = -4$ | 0~+85℃ | Unit |
|                                  |                 |      |                                                     | 10          | Unit | min. | typ.   | max.    | mın.       | max.   |      |
|                                  |                 | 4.5  |                                                     |             |      |      |        |         |            |        |      |
| Input HIGH voltage               | Vih             | 5    |                                                     |             |      | 2.0  |        | -       | 2.0        |        | V    |
|                                  |                 | 5. 5 |                                                     |             |      |      |        |         |            |        |      |
|                                  |                 | 4.5  |                                                     |             |      |      |        |         |            |        |      |
| Input LOW voltage                | $V_{1L}$        | 5    |                                                     |             |      |      |        | 0.8     |            | 0.8    | V    |
|                                  |                 | 5. 5 |                                                     |             |      |      |        |         |            |        |      |
| Output HIGH voltage              | V <sub>он</sub> | 4.5  | V <sub>1H</sub><br>or                               | -20.0       | μΑ   | 4.4  | 4.5    |         | 4.4        |        | V    |
|                                  |                 | 4.5  | VII                                                 | - 6.0       | mA   | 3.86 |        |         | 3.76       |        | V    |
| Output LOW voltage               | $V_{OL}$        | 4.5  | V <sub>IH</sub><br>or                               | 20. 0       | μA   |      | 0.0    | 0. 1    |            | 0.1    | V    |
| 3                                | . 02            | 4.5  | VIL                                                 | 6. 0        | mA   |      |        | 0. 32   |            | 0.37   | V    |
| Input current                    | Iı              | 5.5  | V <sub>1</sub> =V <sub>C</sub>                      | or GND      |      |      |        | ±0.1    |            | ±0.1   | μA   |
| 3-state output off state current | Ioz             | 5. 5 | $V_1 = V_{1H}$ or $V_{11}$<br>$V_0 = V_{CC}$ or GND |             |      |      |        | ±0.5    |            | ±0.5   | μΑ   |
| Quiescent supply current         | $I_{CC}$        | 5. 5 | $V_1 = V_{CC}$ or GND, $I_0 = 0$                    |             |      |      |        | 8. 0    |            | 80. 0  | μA   |

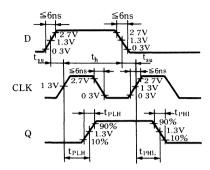
# ■ AC Characteristics (GND=0V, Input transition time ≤6ns, C<sub>L</sub>=50pF)

|                                 |                  |                     |                    |      | T      | emperat | ure         |        |      |
|---------------------------------|------------------|---------------------|--------------------|------|--------|---------|-------------|--------|------|
| Parameter                       | Symbol           | V <sub>CC</sub> (V) | Test Conditions    | -    | Γa=25℃ |         | $T_a = -40$ | )~+85℃ | Unit |
|                                 |                  | (*/                 |                    | min. | typ.   | max.    | min.        | max.   |      |
| Output rise time                | t <sub>TLH</sub> | 4. 5                |                    |      | 8      | 15      |             | 19     | ns   |
| Output fall time                | t <sub>THL</sub> | 4. 5                |                    |      | 6      | 15      |             | 19     | ns   |
| Propagation time<br>CLK→Q (L→H) | t <sub>PLH</sub> | 4. 5                |                    |      | 15     | 30      |             | 38     | ns   |
| Propagation time<br>CLK→Q (H→L) | t <sub>PHL</sub> | 4.5                 |                    |      | 16     | 30      |             | 38     | ns   |
| 3-state propagation time (H→Z)  | t <sub>PHZ</sub> | 4. 5                | $R_L = 1 k \Omega$ |      | 16     | 20      |             | 25     | ns   |
| 3-state propagation time (L→Z)  | tPLZ             | 4. 5                | $R_L = 1 k \Omega$ |      | 15     | 20      |             | 25     | ns   |
| 3-state propagation time (Z→H)  | tрzн             | 4. 5                | $R_L = 1 k\Omega$  |      | 14     | 20      |             | 25     | ns   |
| 3-state propagation time (Z→L)  | tPZL             | 4. 5                | $R_L=1 k \Omega$   |      | 14     | 20      |             | 25     | ns   |
| Minimum Set-up time             | t <sub>su</sub>  | 4.5                 |                    |      | 2      | 20      |             | 25     | ns   |
| Minimum Hold time               | t <sub>h</sub>   | 4.5                 |                    |      | _      | 0       |             |        | ns   |
| Maximum clock frequency         | $f_{max}$        | 4.5                 |                    | 30   | 87     |         | 24          |        | MHz  |

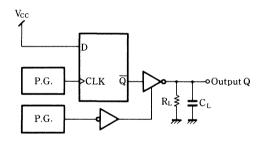
- Switching Time Measuring Circuit and Waveforms
- [1]  $t_{TLH}$ ,  $t_{THL}$ ,  $t_{SU}$ ,  $t_{PML}$ ,  $t_{PHL}$  ( $CLK \rightarrow Q$ )
  - 1. Measuring Circuit



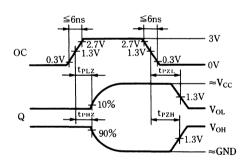
### 2. Waveforms



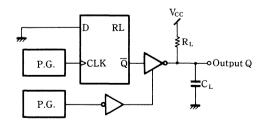
- (2) tpHZ, tpZH
  - 1. Measuring Circuit



### 2. Waveforms



- [3]  $t_{PLZ}$ ,  $t_{PZL}$ 
  - 1. Measuring Circuit



### 2. Waveforms

See above [2] 2. for waveforms.



# MN74HC4305/MN74HC4305S

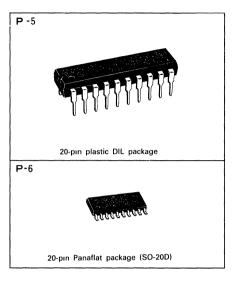
# TTL Input Octal TRI-STATE Inverting Buffers

### **■** Description

MN74HC4305/MN74HC4305S are TTL input octal tri-state inverting buffer.

All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more is logic "1". Large current output makes possible high-speed operation for driving a large capacity busline. It has input  $1\overline{G}$  and  $2\overline{G}$  where output becomes enabled at LOW, and each can control 4 buffers.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND to protect the input/output from damage by static electricity.



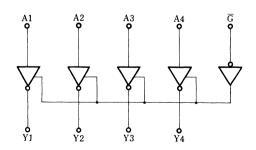
### ■ Truth Table

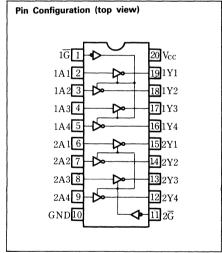
| In                          | put | Output | In  | Output |      |  |
|-----------------------------|-----|--------|-----|--------|------|--|
| 1 $\overline{\overline{G}}$ | 1 A | 1 Y    | 2 G | 2 A    | 2 Y  |  |
| L                           | L   | Н      | L   | L      | Н    |  |
| L                           | Н   | L      | L   | Н      | L    |  |
| Н                           | L   | Hi-Z   | Н   | L      | Hi-Z |  |
| Н                           | Н   | Hi-Z   | Н   | Н      | Hi-Z |  |

Note:

Hi-Z: High impedance

#### ■ Logic Diagram





# ■ Absolute Maximum Ratings

|                | Parameter           | ٢                            | Symbol                          | Rating                                    | Unit   |
|----------------|---------------------|------------------------------|---------------------------------|-------------------------------------------|--------|
| Supply voltage | ge                  |                              | $V_{\rm cc}$                    | $-0.5 \sim +7.0$                          | V      |
| Input/output   | voltage             |                              | V <sub>I</sub> , V <sub>O</sub> | $-0.5 \sim V_{\rm CC} + 0.5$              | V      |
| Input protec   | tion diode current  |                              | IIK                             | ±20                                       | mA     |
| Output paras   | sitic diode current |                              | Іок                             | ±20                                       | mA     |
| Output curre   | ent                 |                              | Io                              | ±35                                       | mA     |
| Supply curre   | Supply current      |                              |                                 | ± 70                                      | mA     |
| Storage tem    | perature range      |                              | Tstg                            | -65~+150                                  | °C     |
|                | MN74 HC4305         | $Ta = -40 \sim +60^{\circ}C$ | $P_{D}$                         | 400                                       | mW     |
| Power          | MN74 HC4305         | $Ta = +60 \sim +85^{\circ}C$ | Гр                              | Decrease to 200mW at the rate of 8mW/°C   | m vv   |
| dissipation    | MN74 HC4305 S       | $Ta = -40 \sim +60^{\circ}C$ | $P_{D}$                         | 275                                       | mW     |
|                | MIN 4 HC4303 S      | $Ta = +60 \sim +85^{\circ}C$ | rp                              | Decrease to 200mW at the rate of 3.8mW/°C | 111 VV |

# ■ Operating Conditions

| Parameter                   | Symbol                          | Vcc(V) | Rating            | Unit |
|-----------------------------|---------------------------------|--------|-------------------|------|
| Operating supply voltage    | $V_{CC}$                        |        | 4.5~5.5           | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |        | 0~V <sub>CC</sub> | V    |
| Operating temperature range | TA                              |        | -40~+85           | °C   |
| Input rise and fall time    | t <sub>r</sub> ,t <sub>f</sub>  | 4.5    | 0~500             | ns   |

|                                  |          |                | Tes             | st Conditio                                                 | ns        |      | ,       | Tempera | ture  |         |      |
|----------------------------------|----------|----------------|-----------------|-------------------------------------------------------------|-----------|------|---------|---------|-------|---------|------|
| Parameter                        | Symbol   | $V_{CC}$ $(V)$ | Vı              | 7                                                           |           | 7.   | Γa=25°0 | 2       | Ta=-4 | 0~+85°C | Unit |
|                                  |          | ,              | , ,             | Io                                                          | Unit      | min. | typ.    | max.    | min.  | max.    |      |
|                                  |          | 4.5            |                 |                                                             |           |      |         |         |       |         |      |
| Input HIGH voltage               | Vih      | 5              |                 |                                                             |           | 2.0  |         |         | 2.0   |         | V    |
|                                  |          | 5.5            |                 |                                                             |           |      |         |         |       |         |      |
|                                  |          | 4.5            |                 |                                                             |           |      |         |         |       |         |      |
| Input LOW voltage                | $V_{11}$ | 5              |                 |                                                             |           |      |         | 0.8     |       | 0.8     | V    |
|                                  |          | 5.5            |                 |                                                             |           |      |         |         |       |         |      |
| Output HIGH voltage              | Vон      | 4.5            | V <sub>IH</sub> | -20.0                                                       | μA        | 4.4  | 4.5     |         | 4.4   |         | V    |
| Output HIGH voltage              |          | 4.5            | V <sub>11</sub> | - 6.0                                                       | mA        | 3.86 |         |         | 3.76  |         | V    |
| O to the OW stalks as            |          | 4.5            | ViH             | 20.0                                                        | μΑ        |      | 0.0     | 0.1     |       | 0.1     | V    |
| Output LOW voltage               | Vol      | 4.5            | VII             | 6. 0                                                        | mA        |      |         | 0. 32   |       | 0. 37   | V    |
| Input current                    | Iı       | 5.5            | V i=Vcc         | or GND                                                      |           |      |         | ±0.1    |       | ±1.0    | μA   |
| 3-state output off state current | Ioz      | 5. 5           | ļ               | $I = V_{IH} \text{ or } V_{II}$ $0 = V_{CC} \text{ or GND}$ |           |      |         | ±0.5    |       | ± 5.0   | μΑ   |
| Quiescent supply current         | Ioc      | 5. 5           | $V_i = V_C$     | c or GND                                                    | $I_0 = 0$ |      |         | 8. 0    |       | 80. 0   | μA   |

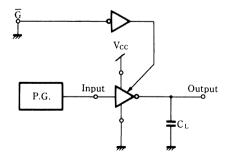


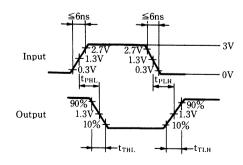
 $\blacksquare$  AC Characteristics (GND=0V, Input transition time  $\leq$ 6ns, C<sub>L</sub>=50pF)

|                                              |        |     |                       |      | Te      | mperatu | re          |       |      |
|----------------------------------------------|--------|-----|-----------------------|------|---------|---------|-------------|-------|------|
| Parameter                                    | Symbol | (V) | Test Conditions       | •    | Γa=25°C |         | $T_a = -40$ | ~+85℃ | Unit |
|                                              |        | (*/ |                       | min. | typ.    | max.    | min.        | max.  |      |
| Minimum Set-up time                          | tтLн   | 4.5 |                       |      | 8       | 15      |             | 19    | ns   |
| Output fall time                             | tTHL   | 4.5 |                       |      | 6       | 15      |             | 19    | ns   |
| Propagation time<br>(L →H)                   | tрLн   | 4.5 |                       |      | 8       | 20      |             | 25    | ns   |
| Propagation time<br>(H→L)                    | tPHL   | 4.5 |                       |      | 8       | 20      |             | 25    | ns   |
| 3-state propagation time<br>(H→Z)            | tрнz   | 4.5 | $R_L = 1 \ k  \Omega$ |      | 12      | 25      |             | 31    | ns   |
| 3-state propagation time $(L \rightarrow Z)$ | tPLZ   | 4.5 | $R_L = 1$ k $\Omega$  |      | 10      | 25      |             | 31    | ns   |
| 3-state propagation time<br>(Z→H)            | tрzн   | 4.5 | $R_L = 1 k \Omega$    |      | 12      | 20      |             | 25    | ns   |
| 3-state propagation time (Z → L)             | tpzL   | 4.5 | $R_L = 1 k\Omega$     |      | 17      | 30      |             | 38    | ns   |

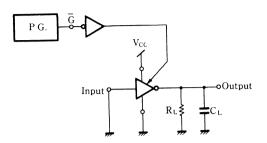
# • Switching Time Measuring Circuit and Waveforms

- (1)  $t_{TLH}$ ,  $t_{THL}$ ,  $t_{PLH}$ ,  $t_{PHL}$ 
  - 1. Measuring Circuit

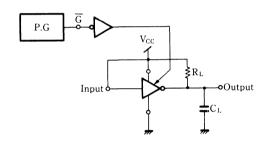


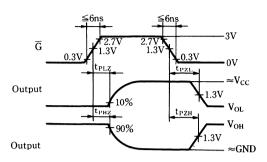


- (2) tphz, tpzh
  - 1. Measuring Circuit



- (3) tplz, tpzL
  - 1. Measuring Circuit





## 2. Waveforms

See above [2] 2. for waveforms.



# MN74HC4306/MN74HC4306S

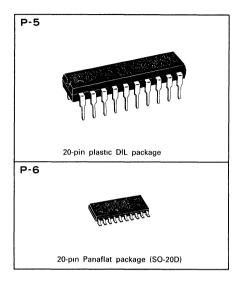
TTL Input Octal TRI-STATE Buffer

#### **■** Description

MN74HC4305/MN74HC4305S are TTL input octal tri-state buffer.

All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more is logic "1". Large current output makes possible high-speed operation for driving a large capacity busline. It has input  $1\overline{G}$  and  $2\overline{G}$  where output becomes enabled at LOW, and each can control 4 buffers.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND to protect the input/output from damage by static electricity.



#### **■** Truth Table

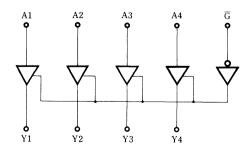
| In  | out | Output | Inj | Output |      |
|-----|-----|--------|-----|--------|------|
| 1 G | 1 A | 1 Y    | 2 G | 2 A    | 2 Y  |
| L   | L   | L      | L   | L      | L    |
| L   | Н   | Н      | L   | Н      | Н    |
| Н   | L   | Hi-Z   | Н   | L      | Hi-Z |
| Н   | Н   | Hi-Z   | Н   | Н      | Hi-Z |

Note:

Hi-Z: High impedance

# 

#### **■** Logic Diagram



# ■ Absolute Maximum Ratings

|                | Paramete                                         | r            | Symbol                             | Rating                                    | Unit            |          |                              |   |
|----------------|--------------------------------------------------|--------------|------------------------------------|-------------------------------------------|-----------------|----------|------------------------------|---|
| Supply voltage | ge                                               | ;            |                                    | $-0.5 \sim +7.0$                          | V               |          |                              |   |
| Input/output   | nput/output voltage                              |              |                                    | out/output voltage                        |                 |          | $-0.5 \sim V_{\rm CC} + 0.5$ | V |
| Input protec   | ion diode current                                |              | tion diode current                 |                                           | I <sub>IK</sub> | ±20      | mA                           |   |
| Output paras   | itic diode current                               |              | Іок                                | ±20                                       | mA              |          |                              |   |
| Output curre   | Output current                                   |              | Io                                 | ± 35                                      | mA              |          |                              |   |
| Supply curre   | nt                                               |              | I <sub>CC</sub> , I <sub>GND</sub> | ± 70                                      | mA              |          |                              |   |
| Storage temp   | perature range                                   | rature range |                                    | rature range                              |                 | -65~+150 | $^{\circ}$                   |   |
|                | MN74 HC 4306 Ta=−40~+60°C                        |              | $P_{D}$                            | 400                                       | mW              |          |                              |   |
| Power          | T160 105°0                                       |              | l ro                               | Decrease to 200mW at the rate of 8mW/°C   | 111 44          |          |                              |   |
| dissipation    | dissipation MN74 HC4306S $Ta=-40\sim+60^{\circ}$ |              | $P_{D}$                            | 275                                       | mW              |          |                              |   |
|                | $T_a = +60 \sim +85^{\circ}$                     |              | l rp                               | Decrease to 200mW at the rate of 3.8mW/°C | III VV          |          |                              |   |

# ■ Operating Conditions

| Parameter                   | Symbol                          | V <sub>CC</sub> (V) | Rating            | Unit |
|-----------------------------|---------------------------------|---------------------|-------------------|------|
| Operating supply voltage    | Vcc                             |                     | 4.5~5.5           | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |                     | 0~V <sub>cc</sub> | V    |
| Operating temperature range | TA                              |                     | -40~+85           | °    |
| Input rise and fall time    | tr, tf                          | 4.5                 | 0~500             | ns   |

# ■ DC Characteristics (GND=0V)

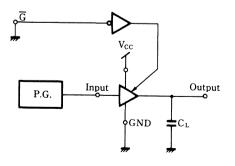
|                                  |          |       | Tes                   | st Conditio | ns   |      | T      | emperat | ure  |        |      |
|----------------------------------|----------|-------|-----------------------|-------------|------|------|--------|---------|------|--------|------|
| Parameter                        | Symbol   | (V)   | V <sub>1</sub>        | Io          |      |      | Ta=25℃ |         |      | ~+85°C | Unit |
|                                  |          | ( • ) |                       | 10          | Unit | min. | typ.   | max.    | min. | max.   |      |
|                                  |          | 4.5   |                       |             |      |      |        |         |      |        |      |
| Input HIGH voltage               | Vih      | 5     |                       |             |      | 2.0  |        |         | 2.0  |        | V    |
|                                  |          | 5.5   |                       |             |      |      |        |         |      |        |      |
|                                  |          | 4.5   |                       |             |      |      |        |         |      |        |      |
| Input LOW voltage                | $V_{1L}$ | 5     |                       |             |      |      |        | 0.8     |      | 0.8    | V    |
|                                  |          | 5.5   |                       |             |      |      |        |         |      |        |      |
|                                  |          | 4.5   | VIH                   | -20.0       | μA   | 4.4  | 4.5    |         | 4.4  |        | V    |
| Output HIGH voltage              | Vон      | 4.5   | or<br>V <sub>IL</sub> | - 6.0       | mA   | 3.86 |        |         | 3.76 |        | V    |
|                                  |          | 4.5   | VIH                   | 20. 0       | μΑ   |      | 0.0    | 0.1     |      | 0. 1   | V    |
| Output LOW voltage               | Vol      | 4.5   | or<br>V <sub>IL</sub> | 6. 0        | mA   |      |        | 0.32    |      | 0.37   | V    |
| Input current                    | Iı       | 5.5   | V 1=Vc                | or GND      |      |      |        | ±0.1    |      | ±1.0   | μA   |
| 3-state output off state current | Ioz      | 5.5   | 1                     | IH OF VIL   |      |      |        | ±0.5    |      | ±5.0   | μΑ   |
| Quiescent supply current         | Icc      | 5.5   |                       | c or GND    |      |      |        | 8. 0    |      | 80. 0  | μA   |

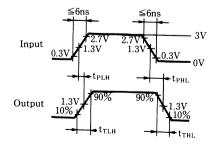


 $\blacksquare$  AC Characteristics (GND=0V, Input transition time  $\leq$ 6ns, C<sub>L</sub>=50pF)

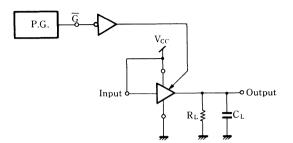
|                                |                  |       |                      |      | Τe     | mperat | ure    |        |      |
|--------------------------------|------------------|-------|----------------------|------|--------|--------|--------|--------|------|
| Parameter                      | Symbol           | (V)   | Test Conditions      | -    | Γa=25℃ |        | Ta=-40 | )~+85℃ | Unit |
|                                |                  | ( • / |                      | min. | typ.   | max.   | min.   | max.   |      |
| Output rise time               | t <sub>TLH</sub> | 4.5   |                      |      | 8      | 15     |        | 19     | ns   |
| Output fall time               | tTHL             | 4.5   |                      |      | 6      | 15     |        | 19     | ns   |
| Propagation time<br>(L→H)      | tрLн             | 4.5   |                      |      | 8      | 20     |        | 25     | ns   |
| Propagation time<br>(H→L)      | t <sub>PHL</sub> | 4.5   |                      |      | 12     | 20     |        | 25     | ns   |
| 3-state propagation time (H→Z) | tPHZ             | 4.5   | $R_L = 1  k  \Omega$ |      | 14     | 25     |        | 31     | ns   |
| 3-state propagation time (L→Z) | tPLZ             | 4.5   | $R_L = 1 k\Omega$    |      | 14     | 25     |        | 31     | ns   |
| 3-state propagation time (Z→H) | tрzн             | 4.5   | $R_L = 1 k\Omega$    |      | 10     | 20     |        | 25     | ns   |
| 3-state propagation time (Z→L) | tPZL             | 4.5   | $R_L = 1 k\Omega$    |      | 14     | 25     |        | 31     | ns   |

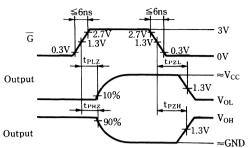
- Switching Time Measuring Circuit and Waveforms
- (1) ttlh, tthl, tplh, tphl
  - 1. Measuring Circuit



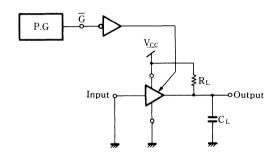


- [2] tphz, tpzh
  - 1. Measuring Circuit





- (3) tPLZ, tPZL
- 1. Measuring Circuit



# 2. Waveforms

See above [2] 2. for waveforms.

# MN74HC4520/MN74HC4520S

# Dual Binary Up Counter

#### ■ Description

MN74HC4520/MN74HC4520S contain independent dual 4-bit binary up counters.

It is counted by the rise of CLK, when  $\overline{\text{CLK}}$  is "H" and counted by the fall of CLK, when  $\overline{\text{CLK}}$  is "L". When clear input is "H", it clears the counter regardless of clock and all outputs (Q0 $\sim$ Q3) is "L".

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.

#### ■ Truth Table

| CLK     | CLK | CLR | Mode                |
|---------|-----|-----|---------------------|
| ×       | ×   | Н   | All outputs are low |
| £       | Н   | L   | Counter Advances    |
| L       | عر_ | L   | Counter Advances    |
| <u></u> | ×   | L   | No Change           |
| ×       | 7   | L   | No Change           |
| 1       | L   | L   | No Change           |
| Н       | 74  | L   | No Change           |

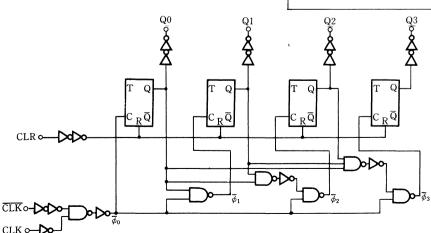
#### Note:

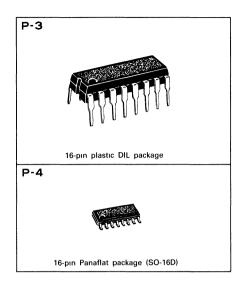
1. ×: Either HIGH or LOW; it doesn't matter

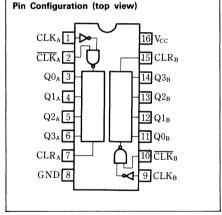
2. The fall of clock from "H" to "L"

3. 1: The rise of clock from "L" to "H"

# ■ Logic Diagram







# ■ Absolute Maximum Ratings

|              | Paramete                                     | r            | Symbol                             | Rating                                    | Unit   |                     |                              |   |
|--------------|----------------------------------------------|--------------|------------------------------------|-------------------------------------------|--------|---------------------|------------------------------|---|
| Supply volta | ge                                           |              | $V_{CC}$                           | $-0.5 \sim +7.0$                          | V      |                     |                              |   |
| Input/output | put/output voltage                           |              |                                    | out/output voltage                        |        |                     | $-0.5 \sim V_{\rm CC} + 0.5$ | V |
| Input protec | ection diode current                         |              | I <sub>IK</sub>                    | ±20                                       | mA     |                     |                              |   |
| Output paras | Output parasitic diode current               |              |                                    | $\pm 20$                                  | mA     |                     |                              |   |
| Output curre | Output current                               |              | Io                                 | ±25                                       | mA     |                     |                              |   |
| Supply curre | ent                                          |              | I <sub>CC</sub> , I <sub>GND</sub> | ±50                                       | mA     |                     |                              |   |
| Storage tem  | perature range                               | rature range |                                    | erature range                             |        | <del>-65~+150</del> | $^{\circ}$ C                 |   |
|              | MN74 HC4520 Ta=−40~+60°C                     |              | $P_{D}$                            | 400                                       | mW     |                     |                              |   |
| Power        | Power $Ta=+60\sim+85^{\circ}$                |              | LD                                 | Decrease to 200mW at the rate of 8mW/°C   | III VV |                     |                              |   |
| dissipation  | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1        |              | $P_{\mathrm{D}}$                   | 275                                       | W      |                     |                              |   |
|              | MN74 HC4520S $T_a = +60 \sim +85 ^{\circ}$ C |              | l rp                               | Decrease to 200mW at the rate of 3.8mW/°C | mW     |                     |                              |   |

# ■ Operating Conditions

| Parameter                   | Symbol                          | V <sub>CC</sub> (V) | Rating            | Unit |
|-----------------------------|---------------------------------|---------------------|-------------------|------|
| Operating supply voltage    | $V_{CC}$                        |                     | 1.4~6.0           | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |                     | 0~V <sub>cc</sub> | V    |
| Operating temperature range | TA                              |                     | -40~+85           | °C   |
|                             |                                 | 2.0                 | 0~1000            | ns   |
| Input rise and fall time    | t <sub>r</sub> , t <sub>f</sub> | 4.5                 | 0~500             | ns   |
|                             |                                 | 6.0                 | 0~400             | ns   |

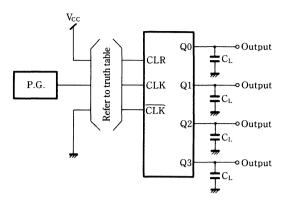
# ■ DC Characteristics (GND=0V)

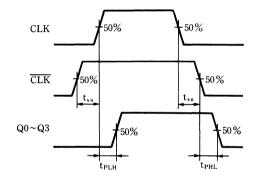
|                          |          |     | Te                      | st Condition | ons                  |      | T      | emperatı | ıre    |       |      |
|--------------------------|----------|-----|-------------------------|--------------|----------------------|------|--------|----------|--------|-------|------|
| Parameter                | Symbol   | (V) | Vı                      | Io           |                      | •    | Γa=25° | 2        | Ta=-40 | ~+85℃ | Unit |
|                          |          | (•, | VI                      | 10           | Unit                 | min. | typ.   | max.     | min.   | max.  |      |
|                          |          | 2.0 |                         |              |                      | 1.5  |        |          | 1.5    |       |      |
| Input HIGH voltage       | $V_{IH}$ | 4.5 |                         |              |                      | 3.15 |        |          | 3.15   |       | V    |
|                          |          | 6.0 |                         |              |                      | 4.2  |        |          | 4.2    |       |      |
|                          |          | 2.0 |                         |              |                      |      |        | 0.3      |        | 0.3   |      |
| Input LOW voltage        | $V_{II}$ | 4.5 |                         |              |                      |      |        | 0.9      |        | 0.9   | V    |
|                          |          | 6.0 |                         |              |                      |      |        | 1.2      |        | 1.2   |      |
|                          |          | 2.0 |                         | -20.0        | μA                   | 1.9  | 2.0    |          | 1.9    |       |      |
|                          |          | 4.5 | VIH                     | -20.0        | μA                   | 4.4  | 4.5    |          | 4.4    |       |      |
| Output HIGH voltage      | $V_{OH}$ | 6.0 | or                      | -20.0        | μA                   | 5.9  | 6.0    |          | 5.9    |       | V    |
|                          |          | 4.5 | VIH                     | -4.0         | mA                   | 3.86 |        |          | 3.76   |       |      |
|                          |          | 6.0 |                         | -5.2         | mA                   | 5.36 |        |          | 5.26   |       |      |
|                          |          | 2.0 |                         | 20.0         | μA                   |      | 0.0    | 0.1      |        | 0.1   |      |
|                          |          | 4.5 | VIH                     | 20.0         | μA                   |      | 0.0    | 0.1      |        | 0.1   |      |
| Output LOW voltage       | Vol      | 6.0 | or                      | 20.0         | μA                   |      | 0.0    | 0.1      |        | 0.1   | V    |
|                          |          | 4.5 | VIL                     | 4.0          | mA                   |      |        | 0.32     |        | 0.37  |      |
|                          |          | 6.0 |                         | 5.2          | mA                   |      |        | 0.32     |        | 0.37  |      |
| Input current            | Iı       | 6.0 | $V_I = V_C$             | c or GNI     | D                    |      |        | ±0.1     |        | ±1.0  | μΑ   |
| Quiescent supply current | $I_{CC}$ | 6.0 | $V_{\rm I} = V_{\rm C}$ | c or GNI     | D, I <sub>0</sub> =0 |      |        | 8.0      |        | 80.0  | μA   |

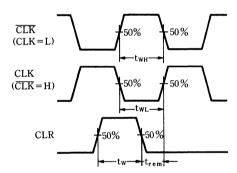
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C<sub>L</sub>=50pF)

|                                                                    |                    | Ves |                 |      |        | emperat |       |        | Unit  ns  ns  ns  ns  ns  ns |
|--------------------------------------------------------------------|--------------------|-----|-----------------|------|--------|---------|-------|--------|------------------------------|
| Parameter                                                          | Symbol             | (V) | Test Conditions |      | Ta=25℃ | ;       | Ta=-4 | 0~+85℃ | Unit                         |
|                                                                    |                    | ` ′ |                 | min. | typ.   | max.    | min.  | max.   |                              |
|                                                                    |                    | 2.0 |                 |      |        | 75      |       | 95     |                              |
| Output rise time                                                   | <b>t</b> TLH       | 4.5 |                 |      | 8      | 15      |       | 19     | ns                           |
|                                                                    |                    | 6.0 |                 |      |        | 13      |       | 16     |                              |
| Į                                                                  |                    | 2.0 |                 |      |        | 75      |       | 95     |                              |
| Output fall time                                                   | <b>t</b> THL       | 4.5 |                 |      | 6      | 15      |       | 19     | ns                           |
|                                                                    |                    | 6.0 | ···             |      |        | 13      |       | 16     |                              |
| Propagation time                                                   |                    | 2.0 |                 |      |        | 175     |       | 220    |                              |
| CLK, $\overline{\text{CLK}} \rightarrow Q_0 (L \rightarrow H)$     | <b>t</b> PLH       | 4.5 |                 |      |        | 35      |       | 44     | ns                           |
|                                                                    |                    | 6.0 |                 |      |        | 30      |       | 37     |                              |
| Propagation time                                                   |                    | 2.0 |                 |      |        | 175     |       | 220    |                              |
| $CLK \rightarrow \overline{CLK} \rightarrow Q_0 (H \rightarrow L)$ | t <sub>PHL</sub>   | 4.5 |                 |      |        | 35      |       | 44     | ns                           |
| OER OER QUAL E                                                     |                    | 6.0 |                 |      |        | 30      |       | 37     |                              |
| Propagation time                                                   |                    | 2.0 |                 |      |        | 250     |       | 315    |                              |
| CLK, $\overline{CLK} \rightarrow Q_3(L \rightarrow H)$             | <b>t</b> PLH       | 4.5 |                 |      |        | 50      |       | 63     | ns                           |
| CLK, CLK → Q3 (L→II)                                               |                    | 6.0 |                 |      |        | 43      |       | 54     |                              |
| Propagation time                                                   |                    | 2.0 |                 |      |        | 250     |       | 315    |                              |
| CLK, <del>CLK</del> →Q <sub>3</sub> (H→L)                          | <b>t</b> PHL       | 4.5 |                 |      |        | 50      |       | 63     | ns                           |
| CLK, CLK 'Q3 (II 'L)                                               |                    | 6.0 |                 |      |        | 43      |       | 54     |                              |
| Propagation time                                                   |                    | 2.0 |                 | 1    |        | 150     |       | 190    |                              |
| CLR→Q <sub>3</sub> (H→L)                                           | t <sub>PHL</sub> . | 4.5 |                 |      |        | 30      |       | 38     | ns                           |
| OLK (43 (H · L)                                                    |                    | 6.0 |                 |      |        | 26      |       | 33     |                              |
| Low level                                                          |                    | 2.0 |                 |      |        | 100     |       | 125    |                              |
| Minimum pulse width                                                | twl                | 4.5 |                 |      |        | 20      |       | 25     | ns                           |
| CLK                                                                |                    | 6.0 |                 |      |        | 17      |       | 21     |                              |
| High level                                                         |                    | 2.0 |                 |      |        | 100     |       | 125    |                              |
| Minimum pulse width                                                | twn                | 4.5 |                 |      |        | 20      |       | 25     | ns                           |
| CLK                                                                |                    | 6.0 |                 |      |        | 17      |       | 21     |                              |
| Minimum pulse width                                                |                    | 2.0 |                 |      |        | 150     |       | 190    |                              |
| CLR                                                                | twcp               | 4.5 |                 |      |        | 30      |       | 38     | ns                           |
| CLK                                                                |                    | 6.0 |                 |      |        | 26      |       | 33     |                              |
| Minimum Set-up time                                                |                    | 2.0 |                 |      |        | 75      |       | 95     |                              |
| CLK→CLK                                                            | tsu                | 4.5 |                 |      |        | 15      |       | 19     | ns                           |
| CLK→CLK                                                            |                    | 6.0 |                 |      |        | 13      |       | 16     |                              |
| Minimum Set-up time                                                |                    | 2.0 |                 |      |        | 50      |       | 65     |                              |
|                                                                    | tsu                | 4.5 |                 |      |        | 10      |       | 13     | ns                           |
| <u>CLK</u> → CLK                                                   |                    | 6.0 |                 |      |        | 9       |       | 11     |                              |
|                                                                    |                    | 2.0 |                 |      |        | 75      |       | 95     |                              |
| Minimum recovery time                                              | trem               | 4.5 |                 |      |        | 15      |       | 19     | ns                           |
|                                                                    |                    | 6.0 |                 |      |        | 13      |       | 16     |                              |
|                                                                    |                    | 2.0 |                 | 6    |        |         | 4     |        |                              |
| Maximum clock frequency                                            | f <sub>max</sub>   | 4.5 |                 | 30   |        |         | 24    |        | MH                           |
|                                                                    |                    | 6.0 |                 | 35   |        |         | 28    |        |                              |

- Switching Time Measuring Circuit and Waveforms
  - 1. Measuring Circuit







# MN74HC40104/MN74HC40104S

4-Bit TRI-STATE Bidirectional Universal Shift Register

#### ■ Description

MN74HC40104/MN74HC40104S are 4-bit 3-state bidirectional shift registers with parallel inputs, parallel outputs, right-shift and left-shift serial inputs, and operational mode control inputs.

Large current output makes possible high-speed operation for driving a large capacity busline.

For sysnchronized-parallel loads, 4-bit data are added to the parallel input, when both mode control inputs (S0 and S1) are HIGH.

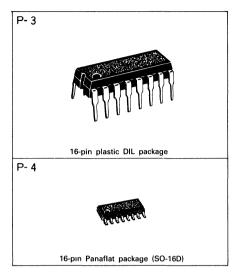
Data are loaded to the respective flip-flops, and are transferred to the outut on the positive going edge of the clock pulse.

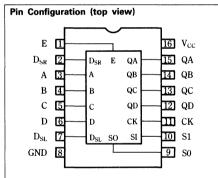
The serial-shift function can be stopped between parallel loads. The right shift functions (when mode-control input S0 is HIGH and S1 is LOW) when there is synchronization to the rise of the clock pulse.

When S0 is LOW and S1 is HIGH, the left shift functions as a result of insertion of new data to the left-shift serial input.

When S0 is LOW and S1 is LOW, all outputs become LOW regardless of the clock pulse.

When enable input is LOW, all outputs become high impedance. Adoption of a silicon gate CMOS process has made possible low power dissipation, high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.





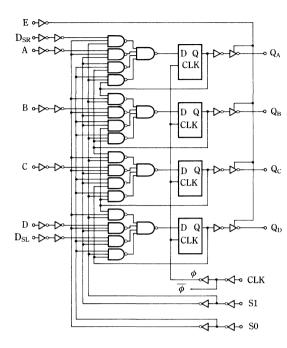
#### ■ Truth Table

|        | Input |     |       |                            |                            |   |     |       |   |          | Out               | put               |          |
|--------|-------|-----|-------|----------------------------|----------------------------|---|-----|-------|---|----------|-------------------|-------------------|----------|
| Enable | Mo    | ode | Clock | Sei                        | rial                       |   | Par | allel |   | 0        | 0                 | 0                 | 0        |
| Е      | S1    | S0  | Clock | $\mathrm{D}_{\mathrm{SL}}$ | $\mathrm{D}_{\mathrm{SR}}$ | A | В   | С     | D | $Q_A$    | $Q_{B}$           | $Q_{C}$           | $Q_D$    |
| L      | ×     | ×   | ×     | ×                          | ×                          | × | ×   | ×     | × | Hi-Z     | Hi-Z              | Hi-Z              | Hi-Z     |
| H      | ×     | ×   | L     | ×                          | ×                          | × | ×   | ×     | × | $Q_{Ao}$ | $Q_{\mathrm{Bo}}$ | $Q_{Co}$          | $Q_{Do}$ |
| Н      | Н     | Н   | 5     | ×                          | ×.                         | a | b   | с     | d | a        | b                 | С                 | d        |
| H      | L     | Н   | 5     | ×                          | Н                          | × | ×   | ×     | × | H        | $Q_{An}$          | $Q_{Bn}$          | $Q_{Cn}$ |
| H      | L     | Н   | 5     | ×                          | L                          | × | ×   | ×     | × | L        | $Q_{An}$          | $Q_{Bn}$          | $Q_{Cn}$ |
| H      | Н     | L   | 5     | Н                          | ×                          | × | ×   | ×     | × | $Q_{Bn}$ | $Q_{Cn}$          | $Q_{Dn}$          | Н        |
| Н      | Н     | L   | 5     | L                          | ×                          | × | ×   | ×     | × | $Q_{Bn}$ | Q <sub>Cn</sub>   | $Q_{\mathrm{Dn}}$ | L        |
| Н      | L     | L   | ×     | ×                          | ×                          | × | ×   | ×     | × | L        | L                 | L                 | L        |

Note:

- 1. 1. Data input is transferred to output on the positive-going edge from LOW to HIGH of the clock
- 2. X: Either HIGH or LOW; it doesn't matter
- 3. Hi-Z: High impedance

# ■ Logic Diagram



■ Absolute Maximum Ratings

|                               | Paramete                                          | er                           | Symbol                             | Rating                                     | Unıt |  |
|-------------------------------|---------------------------------------------------|------------------------------|------------------------------------|--------------------------------------------|------|--|
| Supply voltage                | ge                                                |                              | V <sub>cc</sub>                    | -0.5~+7.0                                  | V    |  |
| Input/output                  | voltage                                           |                              | V <sub>I</sub> , V <sub>O</sub>    | -0.5~V <sub>CC</sub> +0.5                  | V    |  |
| Input protect                 | ion diode current                                 |                              | $I_{IK}$                           | ±20                                        | mA   |  |
| Output paras                  | itic diode current                                |                              | I <sub>OK</sub>                    | ±20                                        | mA   |  |
| Output current                |                                                   |                              | Io                                 | ±35                                        | mA   |  |
| Supply curre                  | nt                                                |                              | I <sub>CC</sub> , I <sub>GND</sub> | ±70                                        | mA   |  |
| Storage temp                  | oerature range                                    |                              | Tstg                               | -65~+150                                   | °C   |  |
|                               | MN74HC40104                                       | $Ta = -40 \sim +60^{\circ}C$ | D                                  | 400                                        |      |  |
| Power $Ta=+60\sim85^{\circ}C$ |                                                   |                              | $P_{D}$                            | Decrease to 200m Watt the rate of 8mW/°C   | mW   |  |
| dissipation                   | dissipation MN74HC40104S $Ta+-40\sim+60^{\circ}C$ |                              |                                    | 275                                        | mW   |  |
| $Ta = +60 \sim +85^{\circ}C$  |                                                   |                              | P <sub>D</sub>                     | Decrease to 200m Watt the rate of 3.8mW/°C | inw  |  |

**■** Operating Conditions

| Parameter                   | Symbol                          | V <sub>CC</sub> (V) | Rating            | Unit |
|-----------------------------|---------------------------------|---------------------|-------------------|------|
| Operation supply voltage    | V <sub>cc</sub>                 |                     | 1.4~6.0           | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |                     | 0~V <sub>CC</sub> | V    |
| Operating temperature range | T <sub>A</sub>                  |                     | -40~+85           | °C   |
|                             |                                 | 2.0                 | 0~1000            |      |
| Input rise and fall time    | t <sub>r</sub> , t <sub>f</sub> | 4.5                 | 0~500             | ns   |
|                             |                                 | 6.0                 | 0~400             |      |



# ■ DC Characteristics (GND=0V)

|                                  |                 |                        | Tes                | t Condition                                   | ons     |      | T       | emperatu | re     |        |      |
|----------------------------------|-----------------|------------------------|--------------------|-----------------------------------------------|---------|------|---------|----------|--------|--------|------|
| Parameter                        | Symbol          | V <sub>CC</sub><br>(V) | V                  | ,                                             |         |      | Ta=25°C |          | Ta=-40 | ~+85°C | Unit |
|                                  |                 | (*/                    | $V_{I}$            | Io                                            | Unit    | min. | typ.    | max.     | min.   | max.   |      |
|                                  |                 | 2.0                    |                    |                                               |         | 1.5  |         |          | 1.5    |        |      |
| Input HIGH voltage               | $V_{IH}$        | 4.5                    |                    |                                               |         | 3.15 |         |          | 3.15   |        | V    |
|                                  |                 | 6.0                    |                    |                                               |         | 4.2  |         |          | 4.2    |        |      |
|                                  |                 | 2.0                    |                    |                                               |         |      |         | 0.3      |        | 0.3    |      |
| Input LOW voltage                | $V_{IL}$        | 4.5                    |                    |                                               |         |      |         | 0.9      |        | 0.9    | V    |
|                                  |                 | 6.0                    |                    |                                               |         |      |         | 1.2      |        | 1.2    |      |
|                                  |                 | 2.0                    |                    | -20.0                                         | μA      | 1.9  | 2.0     |          | 1.9    |        |      |
|                                  |                 | 4.5                    | V <sub>IH</sub>    | -20.0                                         | μA      | 4.4  | 4.5     |          | 4.4    |        |      |
| Output HIGH voltage              | V <sub>OH</sub> | 6.0                    | or                 | -20.0                                         | μA      | 5.9  | 6.0     |          | 5.9    |        | V    |
|                                  |                 | 4.5                    | V <sub>IL</sub>    | -4.0                                          | mA      | 3.86 |         |          | 3.76   |        |      |
|                                  |                 | 6.0                    |                    | -5.2                                          | mA      | 5.36 |         |          | 5.26   |        |      |
|                                  |                 | 2.0                    |                    | 20.0                                          | μA      |      | 0.0     | 0.1      |        | 0.1    |      |
|                                  |                 | 4.5                    | VIH                | 20.0                                          | μA      |      | 0.0     | 0.1      |        | 0.1    |      |
| Output LOW voltage               | $V_{OL}$        | 6.0                    | or                 | 20.0                                          | μA      |      | 0.0     | 0.1      |        | 0.1    | V    |
|                                  |                 | 4.5                    | V <sub>IL</sub>    | 4.0                                           | mA      |      |         | 0.32     |        | 0.37   |      |
|                                  |                 | 6.0                    |                    | 5.2                                           | mA      |      |         | 0.32     |        | 0.37   |      |
| Input current                    | II              | 6.0                    | V <sub>I</sub> =   | V <sub>CC</sub> or G                          | ND      |      |         | ±0.1     |        | ±1.0   | μA   |
| 3-state output off state current | $I_{oz}$        | 6.0                    |                    | =V <sub>IH</sub> or V<br>V <sub>CC</sub> or G |         |      |         | ±0.5     |        | ±5.0   | μΑ   |
| Quiescent supply current         | $I_{CC}$        | 6.0                    | VI=V <sub>CC</sub> | or GND                                        | $I_0=0$ |      |         | 8.0      |        | 80.0   | μΑ   |

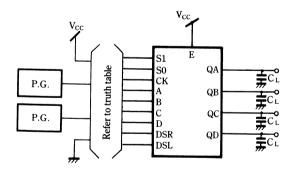
# ■ AC Characteristics (GND=0V, Input transistion tiem $\leq$ 6ns, $C_L$ =50pF)

|                     |                  |                        |                 |      | T       | emperatu | re     |        | J    |
|---------------------|------------------|------------------------|-----------------|------|---------|----------|--------|--------|------|
| Parameter           | Symbol           | V <sub>CC</sub><br>(V) | Test Conditions |      | Ta=25°C |          | Ta=-40 | ~+85°C | Unit |
|                     |                  | (1)                    |                 | min. | tyṗ.    | max.     | min.   | max.   |      |
|                     |                  | 2.0                    |                 |      |         | 75       |        | 95     |      |
| Output rise time    | t <sub>TLH</sub> | 4.5                    |                 |      | 8       | 15       |        | 19     | ns · |
|                     |                  | 6.0                    |                 |      |         | 13       |        | 16     |      |
|                     |                  | 2.0                    |                 |      |         | 75       |        | 95     |      |
| Output fall time    | t <sub>THL</sub> | 4.5                    |                 |      | 6       | 15       |        | 19     | ns   |
|                     |                  | 6.0                    |                 |      |         | 13       |        | 16     |      |
| Propagation time    |                  | 2.0                    |                 |      |         | 150      |        | 190    |      |
| CLŘ→Q4              | t <sub>PLH</sub> | 4.5                    |                 |      |         | 30       |        | 38     | ns   |
| (L→H)               |                  | 6.0                    |                 |      |         | 26       |        | 33     |      |
| Propagation time    |                  | 2.0                    |                 |      |         | 150      |        | 190    |      |
| CLK→Q4              | t <sub>PHL</sub> | 4.5                    |                 |      |         | 30       |        | 38     | ns   |
| (H→L)               |                  | 6.0                    |                 |      |         | 26       |        | 33     |      |
| 3-stage             |                  | 2.0                    |                 |      |         | 175      |        | 220    |      |
| propagation time    | t <sub>HZ</sub>  | 4.5                    | RL=1KΩ          |      |         | 35       |        | 44     | ns   |
| (H→Z)               |                  | 6.0                    |                 |      |         | 30       |        | 37     |      |
| 3-stage             |                  | 2.0                    |                 |      |         | 175      |        | 220    |      |
| propagation time    | t <sub>LZ</sub>  | 4.5                    | RL=1KΩ          |      |         | 35       |        | 44     | ns   |
| $(L \rightarrow Z)$ |                  | 6.0                    |                 |      |         | 30       |        | 37     |      |
| 3-stage             |                  | 2.0                    |                 |      |         | 150      |        | 190    |      |
| propagation time    | t <sub>ZH</sub>  | 4.5                    | RL=1KΩ          |      |         | 30       | ļ      | 38     | ns   |
| (Z→H)               |                  | 6.0                    |                 |      |         | 26       |        | 33     |      |

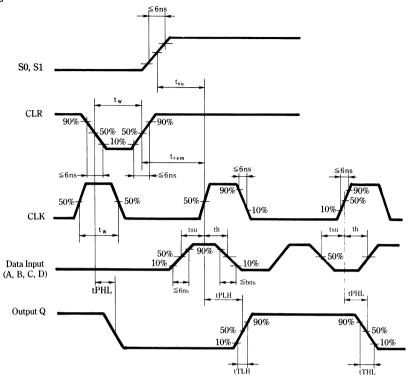
# ■ AC Characteristics (GND=0V, Input transistion tiem $\leq$ 6ns, $C_L$ =50pF)

|                            |                  |                     |                 |      | Т       | emperatu | re     |        |      |
|----------------------------|------------------|---------------------|-----------------|------|---------|----------|--------|--------|------|
| Parameter                  | Symbol           | V <sub>CC</sub> (V) | Test Conditions |      | Ta=25°C |          | Ta=-40 | ~+85°C | Unit |
|                            |                  | (,,                 |                 | min. | typ.    | max.     | mın.   | max.   |      |
| 3-stage                    |                  | 2.0                 |                 |      |         | 150      |        | 190    |      |
| propagation time           | $t_{ZL}$         | 4.5                 | RL=1KΩ          |      |         | 30       |        | 38     | ns   |
| $(Z \rightarrow L)$        |                  | 6.0                 |                 |      |         | 26       |        | 33     |      |
|                            |                  | 2.0                 |                 |      |         | 100      |        | 125    |      |
| Minimum pulse width CLK    | tw               | 4.5                 |                 |      |         | 20       |        | 25     | ns   |
| CBIT                       |                  | 6.0                 |                 |      |         | 17       |        | 21     |      |
|                            |                  | 2.0                 |                 |      | }       | 100      |        | 125    |      |
| Mınımum Set-up time        | $t_{su}$         | 4.5                 |                 |      |         | 20       |        | 25     | ns   |
|                            |                  | 6.0                 |                 |      |         | 17       |        | 21     |      |
|                            |                  | 2.0                 |                 |      | _       | 0        |        | 0      |      |
| Minimum Hold time          | t <sub>h</sub>   | 4.5                 |                 |      | _       | 0        |        | 0      | ns   |
|                            |                  | 6.0                 |                 |      | -       | 0        |        | 0      |      |
|                            |                  | 2.0                 |                 |      |         | 125      |        | 155    |      |
| Minimum recovery time      | t <sub>rem</sub> | 4.5                 |                 |      |         | 25       |        | 31     | ns   |
|                            |                  | 6.0                 |                 |      |         | 21       |        | 26     |      |
|                            |                  | 2.0                 |                 | 6    |         |          | 4      |        |      |
| Maximum clock<br>frequency | f <sub>max</sub> | 4.5                 |                 | 30   |         |          | 24     |        | MHz  |
|                            |                  | 6.0                 |                 | 35   |         |          | 28     |        |      |

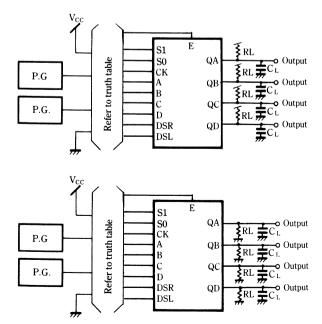
# 1. Measuring Circuit (t<sub>PLH</sub>,t<sub>PHL</sub>)

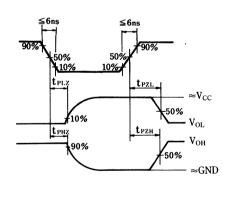






- Switching Time Measuring Circuit and Waveforms
  - 1. Measuring Circuit





# MN74HCT40104/MN74HCT40104S

4-Bit TRI-STATE Bidirectional Universal Shift Register (TTL Input)

## Description

MN74HCT40104/MN74HCT40104S are TTL input level 4-bit 3-state bidirectional shift registers with parallel inputs, parallel outputs, right-shift and left-shift serial inputs, and operational mode-control inputs.

Large current output makes possible for driving a large capacity bus line.

For synchronized-parallel loads, 4-bit data are added to the parallel input, when both mode control inputs (S0 and S1) are HIGH.

Data are loaded to the respective flip-flops, and are transferred to the output at the positive going edge of the clock pulse.

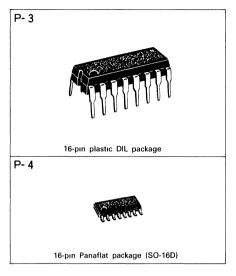
The serial-shift function can be stopped between parallel loads. The right shift functions (when mode-control input S0 is HIGH and S1 is LOW) when there is synchronization to the rise of the clock pulse.

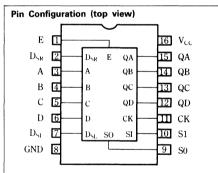
Whe S0 is LOW and S1 is HIGH, the left shift functions as result of insertion of new data to the left-shift serial input.

When S0 is LOW and S1 is LOW, all outputs become LOW regardless of the clock pulse.

When the enable input is LOW, all outputs become high impedance.

Adoption of a silicon gate CMOS process has made possible low power dissipation, high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in  $V_{\rm CC}$  and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.





#### ■ Truth Table

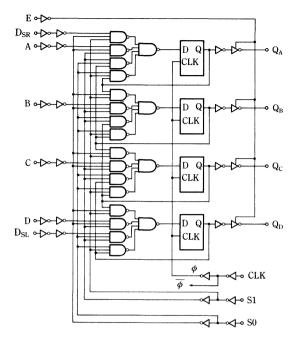
|        | Input |     |       |          |                 |   |     |       |   |          | Out               | put               |                   |
|--------|-------|-----|-------|----------|-----------------|---|-----|-------|---|----------|-------------------|-------------------|-------------------|
| Enable | Mo    | ode | Clock | Se       | erial           |   | Par | allel |   | 0        | 0                 |                   | 0                 |
| Е      | S1    | S0  | Clock | $D_{SL}$ | D <sub>SR</sub> | A | В   | С     | D | $Q_A$    | $Q_{B}$           | $Q_{C}$           | $Q_{\mathrm{D}}$  |
| L      | ×     | ×   | ×     | ×        | ×               | × | ×   | ×     | × | Hı-Z     | Hi-Z              | Hı-Z              | Hi-Z              |
| Н      | ×     | ×   | L     | ×        | ×               | × | ×   | ×     | × | $Q_{Ao}$ | $Q_{\mathrm{Bo}}$ | $Q_{Co}$          | $Q_{\mathrm{Do}}$ |
| Н      | Н     | Н   | 5     | ×        | ×               | a | b   | С     | d | a        | b                 | с                 | d                 |
| Н      | L     | Н   | 5     | ×        | Н               | × | ×   | ×     | × | Н        | $Q_{An}$          | $Q_{Bn}$          | $Q_{Cn}$          |
| Н      | L     | Н   | 5     | ×        | L               | × | ×   | ×     | × | L        | $Q_{An}$          | $Q_{Bn}$          | $Q_{Cn}$          |
| Н      | Н     | L   | 5     | Н        | ×               | × | ×   | ×     | × | $Q_{Bn}$ | $Q_{Cn}$          | $Q_{Dn}$          | Н                 |
| Н      | Н     | L   | 5     | L        | ×               | × | ×   | ×     | × | $Q_{Bn}$ | $Q_{Cn}$          | $Q_{\mathrm{Dn}}$ | L                 |
| H      | L     | L   | ×     | ×        | ×               | × | ×   | ×     | × | L        | L                 | L                 | L                 |

#### Note:

- Data input is transferred to output on the positive-going edge from LOW to HIGH of the clock
- 2. X: Either HIGH or LOW; it doesn't matter.
- 3. Hi-Z: High impedance



# ■ Logic Diagram



■ Absolute Maximum Ratings

|                                   | Paramete                                             | er | Symbol                             | Rating                                     | Unit  |
|-----------------------------------|------------------------------------------------------|----|------------------------------------|--------------------------------------------|-------|
| Supply voltag                     | ge                                                   |    | V <sub>CC</sub>                    | -0.5~+7.0                                  | V     |
| Input/output                      | voltage                                              |    | V <sub>I</sub> , V <sub>O</sub>    | $-0.5 \sim V_{CC} + 0.5$                   | V     |
| Input protect                     | ion diode current                                    |    | I <sub>IK</sub>                    | ±20                                        | mA    |
| Output parasi                     | itic diode current                                   |    | I <sub>OK</sub>                    | ±20                                        | mA    |
| Output current                    |                                                      |    | Io                                 | ±35                                        | mA    |
| Supply curren                     | nt                                                   |    | I <sub>CC</sub> , I <sub>GND</sub> | ±70                                        | mA    |
| Storage temp                      | erature range                                        |    | Tstg                               | −65~+150                                   | °C    |
|                                   | MN74HCT40104 Ta=-40~+60°C                            |    |                                    | 400                                        | mW    |
| Power $Ta = +60 \sim 85^{\circ}C$ |                                                      |    | $P_{\mathrm{D}}$                   | Decrease to 200m Watt the rate of 8mW/°C   | 11144 |
| dissipation                       | lissipation $MN74HCT40104S$ $Ta+-40\sim+60^{\circ}C$ |    |                                    | 275                                        | mW    |
| $Ta = +60 \sim +85^{\circ}C$      |                                                      |    | $P_{D}$                            | Decrease to 200m Watt the rate of 3.8mW/°C | mW    |

# **■** Operating Conditions

| Parameter                   | Symbol                          | V <sub>CC</sub> (V) | Rating            | Unit |
|-----------------------------|---------------------------------|---------------------|-------------------|------|
| Operation supply voltage    | V <sub>cc</sub>                 |                     | 4.5~5.5           | V    |
| Input/output voltage        | V <sub>I</sub> , V <sub>O</sub> |                     | 0~V <sub>CC</sub> | v    |
| Operating temperature range | T <sub>A</sub>                  |                     | -40~+85           | °C   |
| Input rise and fall time    | t <sub>r</sub> , t <sub>f</sub> | 4.5                 | 0~500             | ns   |

# ■ DC Characteristics (GND=0V)

|                                  |          |                     | Tes                | t Conditio                                    | ons       |      | T       | emperatu | re     |        |      |
|----------------------------------|----------|---------------------|--------------------|-----------------------------------------------|-----------|------|---------|----------|--------|--------|------|
| Parameter                        | Symbol   | V <sub>CC</sub> (V) | Vı                 | Ţ                                             |           |      | Ta=25°C |          | Ta=-40 | ~+85°C | Unit |
|                                  |          | (,,                 | V <sub>I</sub>     | I <sub>O</sub>                                | Unit      | mın. | typ.    | max.     | min.   | max.   |      |
|                                  |          | 4.5                 |                    |                                               |           |      |         |          |        |        |      |
| Input HIGH voltage               | $V_{IH}$ | ≀                   |                    |                                               |           | 2.0  |         |          | 2.0    |        | V    |
|                                  |          | 5.5                 |                    |                                               |           |      |         |          |        |        |      |
|                                  |          | 4.5                 |                    |                                               |           |      |         |          |        |        |      |
| Input LOW voltage                | $V_{IL}$ | ≀                   |                    |                                               |           |      |         | 0.8      |        | 0.8    | V    |
|                                  |          | 5.5                 |                    |                                               |           |      |         |          |        |        |      |
|                                  |          | 4.5                 | V <sub>IH</sub>    | -20.0                                         | μA        | 4.4  | 4.5     |          | 4.4    |        |      |
| Output HIGH voltage              | $V_{OH}$ |                     | or                 |                                               |           |      |         |          |        |        | V    |
|                                  |          | 4.5                 | $V_{IL}$           | -4.0                                          | mA        | 3.86 |         |          | 3.76   |        |      |
|                                  |          | 4.5                 | V <sub>IH</sub>    | 20.0                                          | $\mu$ A   |      | 0.0     | 0.1      |        | 0.1    |      |
| Output HIGH voltage              | $V_{OL}$ |                     | or                 |                                               |           |      |         |          |        |        | V    |
|                                  |          | 4.5                 | V <sub>IL</sub>    | 4.0                                           | mA        |      |         | 0.32     |        | 0.37   |      |
| Input current                    | II       | 5.5                 | $V_{I}=$           | V <sub>CC</sub> or G                          | ND        |      |         | ±0.1     |        | ±1.0   | μΑ   |
| 3-state output off state current | $I_{oz}$ | 5.5                 |                    | =V <sub>IH</sub> or V<br>V <sub>CC</sub> or G |           |      |         | ±0.5     |        | ±5.0   | μΑ   |
| Quiescent supply current         | $I_{CC}$ | 5.5                 | VI=V <sub>CC</sub> | or GND                                        | $I_{O}=0$ |      |         | 8.0      |        | 80.0   | μA   |

# ■ AC Characteristics (GND=0V, Input transistion tiem $\leq$ 6ns, $C_L$ =50pF)

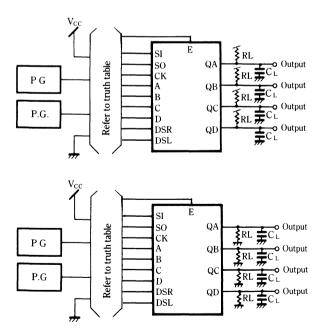
|                                                          |                  |                     |                 |      | Т       | emperatu | re       |        |      |
|----------------------------------------------------------|------------------|---------------------|-----------------|------|---------|----------|----------|--------|------|
| Parameter                                                | Symbol           | V <sub>CC</sub> (V) | Test Conditions |      | Ta=25°C |          | Ta = -40 | ~+85°C | Unit |
|                                                          |                  | . ,                 |                 | min. | typ.    | max.     | mın.     | max.   |      |
| Output rise time                                         | t <sub>TLH</sub> | 4.5                 |                 |      | 8       | 15       |          | 19     | ns   |
| Output fall time                                         | t <sub>THL</sub> | 4.5                 |                 |      | 6       | 15       |          | 19     | ns   |
| Propagation time $CLK \rightarrow Q$ $(L \rightarrow H)$ | t <sub>PLH</sub> | 4.5                 |                 |      |         | 30       |          | 38     | ns   |
| Propagation time<br>CLK→Q<br>(H→L)                       | t <sub>PHL</sub> | 4.5                 |                 |      |         | 30       |          | 38     | ns   |
| 3-stage<br>propagation time<br>(H→Z)                     | t <sub>HZ</sub>  | 4.5                 | RL=1KΩ          |      |         | 35       |          | 44     | ns   |
| 3-stage propagation time $(L\rightarrow Z)$              | t <sub>L.Z</sub> | 4.5                 | RL=1KΩ          |      |         | 35       |          | 44     | ns   |
| 3-stage<br>propagation time<br>(Z→H)                     | t <sub>ZH</sub>  | 4.5                 | RL=1KΩ          |      |         | 30       |          | 38     | ns   |
| 3-stage<br>propagation time<br>(Z→L)                     | tzL              | 4.5                 | RL=1KΩ          |      |         | 30       |          | 38     | ns   |

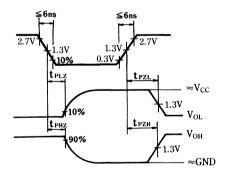


■ AC Characteristics (GND=0V, Input transistion tiem  $\leq$ 6ns,  $C_L$ =50pF)

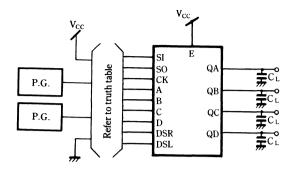
| <u> </u>                   |                  | 3.7                 |                 |      | Т       | emperatu | re       |        |      |
|----------------------------|------------------|---------------------|-----------------|------|---------|----------|----------|--------|------|
| Parameter                  | Symbol           | V <sub>CC</sub> (V) | Test Conditions |      | Ta=25°C |          | Ta = -40 | ~+85°C | Unit |
|                            |                  |                     |                 | min. | typ.    | max.     | min.     | max.   |      |
| Minimum pulse width CLK    | t <sub>w</sub>   | 4.5                 |                 |      |         | 20       |          | 25     | ns   |
| Minimum Set-up time        | t <sub>su</sub>  | 4.5                 |                 |      |         | 20       |          | 25     | ns   |
| Minimum Hold time          | t <sub>h</sub>   | 4.5                 |                 |      |         | 0        |          | 0      | ns   |
| Mınımum recovery time      | t <sub>rem</sub> | 4.5                 |                 |      |         | 25       |          | 31     | ns   |
| Maximum clock<br>frequency | f <sub>max</sub> | 4.5                 |                 | 30   |         |          | 24       |        | MHz  |

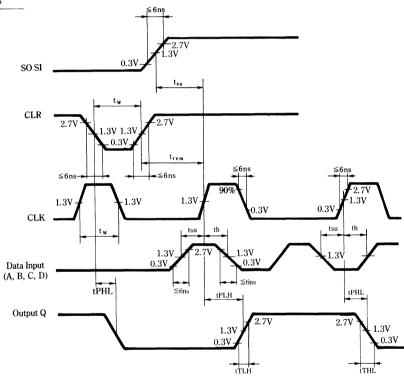
- Switching Time Measuring Circuit and Waveforms
  - 1. Measuring Circuit





# 1. Measuring Circuit (t<sub>PLH</sub>,t<sub>PHL</sub>)







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